Surface participation and dielectric loss in superconducting qubits

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We study the energy relaxation times (T_1) of superconducting transmon qubits in 3D cavities as a function of dielectric participation ratios of material surfaces. This surface participation ratio, representing the fraction of electric field energy stored in a dissipative surface layer, is computed by a two-step finite-element simulation and experimentally varied by qubit geometry. With a clean electromagnetic environment and suppressed non-equilibrium quasiparticle density, we find an approximately proportional relation between the transmon relaxation rates and surface participation ratios. These results suggest dielectric dissipation arising from material interfaces is the major limiting factor for the T_1 of transmons in 3D circuit quantum electrodynamics architecture. Our analysis also supports the notion of spatial discreteness of surface dielectric dissipation. [http://dx.doi.org/10.1063/1.4934486]

Circuit quantum electrodynamics (cQED) systems have emerged as promising platforms for quantum information processing, powered by dramatic improvement of the coherence times of superconducting qubits over the past decade.[1] Such an improvement has been the result of collective efforts in multiple aspects,[2] such as suppression of charge noise and flux noise,[3] better control of the electromagnetic environment,[4] elimination of deposited dielectric materials,[2] development in surface treatment,[5] dilution of surface effects by expanding field volume,[4] and improved filtering and shielding against stray radiation.[6] However, it has been difficult to quantify how much each of these individual measures contribute to the overall improvement. As a result, it remains elusive what the dominant limiting factors are for the coherence of state-of-the-art superconducting qubits such as the 3D and planar transmons.

The superior lifetimes (T_1) of qubits with larger footprints[4] or with more advanced surface preparation[5] strongly suggest the important role of dielectric dissipation[7] from material surfaces. In this letter, we quantitatively extract surface dielectric dissipation in transmon qubits through a combined experimental and numerical study. We find that surface dielectric dissipation is probably still the major limiting factor for T_1 of transmons in 3D cQED architecture, and so far, there is no indication of additional loss mechanisms (up to the level of $Q \sim 10^7$) under our experimental condition. Our analysis also indicates that surface loss for a sub-micrometer area cannot be captured by a uniform loss tangent model, consistent with the hypothesis of discrete dissipation from a small number of microscopic two-level states (TLS).[7–11]

Relaxation of superconducting qubits or resonators can be caused by many dissipative channels such as dielectric loss, conductive loss, and radiation into free space.[2] Dielectric loss can be further decomposed into contributions from various materials or components, so that

$$\frac{1}{T_1} = \frac{\omega}{Q} = \omega \sum_i \frac{p_i}{Q_i} + \Gamma_0, \tag{1}$$

where T_1, Q, and ω are the relaxation time, quality factor (for energy decay), and angular frequency of the qubit or resonator, Γ_0 is the relaxation rate induced by non-dielectric channels, $Q_i = 1/\tan\delta_i$ is the quality factor of the i^{th} material with a dielectric constant of ϵ_i (with $\tan\delta$ known as the loss tangent), and p_i is its participation ratio defined as the fraction of electric field energy stored within the volume of this material.

Crystalline substrates of cQED devices often store a large fraction of electric field energy ($p_i \sim 90\%$), but reportedly show very small loss tangent ($\tan\delta_i < 10^{-6}$ for bulk sapphire[12] and silicon[2]). On the other hand, if a microscopic layer of contaminants such as oxide, adsorbed water, or organics forms at the metal-substrate (MS), substrate-air (SA), and metal-air (MA) interfaces,[13,14] they have much smaller p_i but may still induce significant dissipation with a large $\tan\delta_i$ on the order of 10^{-3}–10^{-2}. Previous studies[15–18] have found a positive correlation between the quality factors of planar resonators and their feature sizes, which can be used to vary p_i. However, a quantitative test of Eq. (1) has been challenging due to the presence of other energy relaxation channels (Γ_0) that have not been fully under control.

Here, we study the energy relaxation time, T_1, of transmon qubits as a function of surface dielectric participation ratio, p_i. Strong suppression of radiation loss is achieved by implementing the 3D cQED architecture[4] where the 3D cavity enclosure provides a clean electromagnetic environment free of spurious modes. The cavity Q and qubit-cavity detuning are sufficiently large to avoid any appreciable Purcell effect. Qubit relaxation due to non-equilibrium quasiparticles can be estimated and suppressed by monitoring and controlling quasiparticle decay time.[19–21] Furthermore, transmons are less sensitive to vortex ac loss than linear resonators because most inductive energy is stored in the Josephson junction rather than the electrodes subjected to vortex penetration. Suppression of these relaxation channels allows us to vary the qubit geometry to change p_i by more than an order of magnitude, making quantitative comparison of surface dielectric loss in different devices viable.

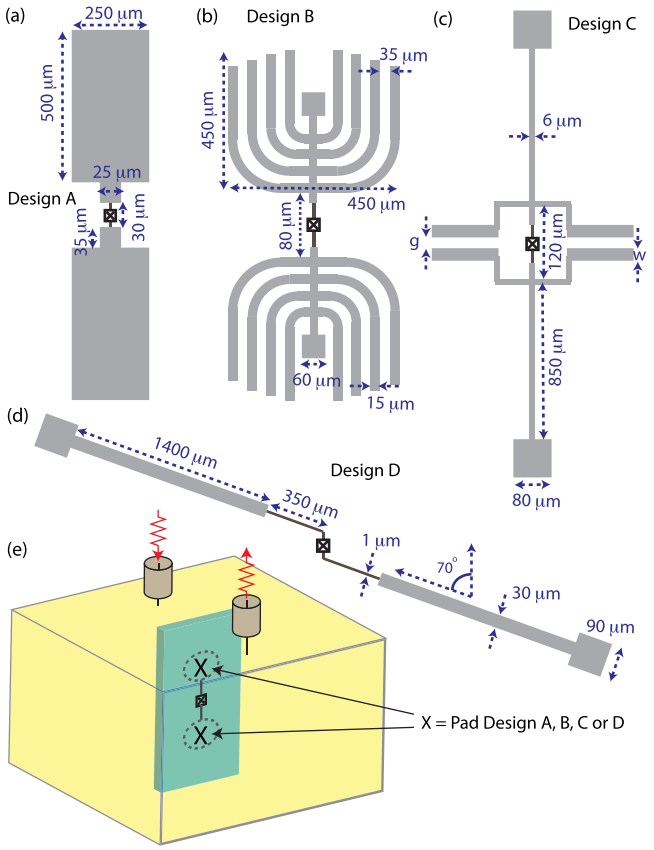

FIG. 1. Geometry of four different designs of transmon qubits used in this study. Most dimensions of the electrodes for each design (A, B, C, and D) are fixed and labeled in respective panels (a)–(d). An exception is that Design C has multiple variations with the dimensions $g = w$ ranging from 1.5 μm to 30 μm. For convenience, we define "leads" as the portion of the electrodes with widths 1 μm or smaller, which only appears in direct connection to the junction in all our designs, as shown in dark brown. The rest of the electrodes wider than 1 μm are called "pads" and are shown in lighter grey. (e) Schematic of the standard 3D cQED setup. Transmon qubits are installed in rectangular waveguide cavities and coupled to the TE101 mode for control and readout.

Each qubit in this study is composed of a single Al/AlO_x/Al Josephson junction and a pair of electrodes forming a shunting capacitor. We report T_1 measured with standard techniques for four different geometric designs of transmons, as shown in Fig. 1. All devices are fabricated on sapphire substrates with identical processes of shadow-mask evaporation and lift-off,[22] and therefore are assumed to have the same loss tangent for the same type of surfaces. All devices have qubit frequency $\omega/2\pi \approx 6$ GHz and cavity frequency $\omega_c/2\pi \approx 9$ GHz.

Full electromagnetic simulation of surface participation ratio of transmon qubits faces significant numerical challenges due to the large span of length scales. One may attempt to model transmon electrodes and any dissipative interface layers as 2D films, and infer p_i from a surface integral of electric field energy. However, such an integral is divergent towards the edge of the films.[23] This divergence is avoided only when the material thicknesses are fully accounted for, as was done in cross-sectional simulations of transmission line resonators.[13,14] Without a similar translational symmetry, a proper calculation of p_i for a transmon qubit generally requires simulation of 3D field distribution in

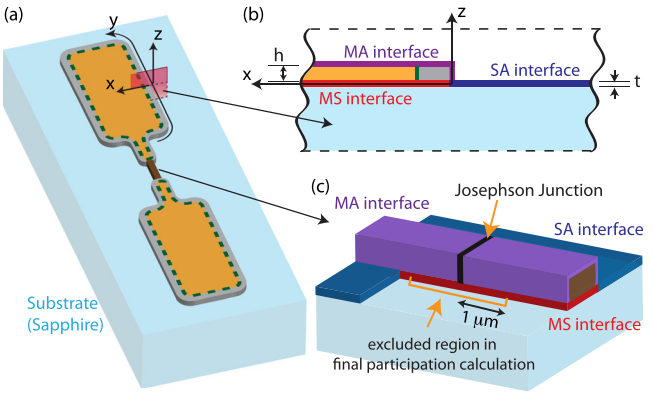

FIG. 2. Illustration of the two-step simulation strategy for computing surface participation ratios. (a) Schematic of a transmon qubit with its electrodes color-coded into several regions. Grey and yellow represent the perimeter and the interior regions of the wide pads of the electrodes, respectively, and brown represents the narrow leads. A global coarse 3D simulation can accurately determine the electric fields across the yellow region, but not in the grey and brown region near the edge of the metal. (b) A cross-section view of the electrode near a metal edge. The electric field distribution within this plane can be computed by a fine 2D simulation. (c) A simplified schematic of the region near the Josephson junction, which is simulated by a local fine 3D simulation. The MA, SA, and MS interfaces are defined in (b) and (c). In our final account of surface participation ratios, contribution from the region within 1 μm from the junction is excluded. All drawings are not to scale.

mm-sized space with sub-nm resolution in critical regions, far exceeding practical computation capacities.

To overcome the numerical challenges, we employ a two-step simulation technique by combining a coarse 3D simulation of the entire qubit-cavity system [Fig. 2(a)] and fine simulations of representative local regions [Figs. 2(b) and 2(c)]. A significant part of the surface participation is associated with regions with highly concentrated electric field such as the edges of the electrodes and the leads near the junction. We argue that the electric field distribution in these regions should have a local scaling property independent of the electromagnetic boundary conditions far away. These scaling properties can be obtained from simulations of local regions with sub-nm resolution and subsequently applied to the global simulation to compute the surface participation ratios.[22] We assume thicknesses of $t = 3$ nm and dielectric constants of $\epsilon = 10$ for all lossy interfaces for easy comparison with a previous simulation of planar resonators.[14] Using different assumptions here would rescale the participation ratios but not change our conclusions qualitatively.

Our simulation shows that a significant contribution to surface participation arises from the region around the junction leads less than 100 nm away from the junction itself [Fig. 3(a)]. This contribution is mostly independent of electrode geometry, and can be dominant for devices with relatively small surface participation.[22] However, if surface dielectric dissipation originates from a discrete set of TLS with density similar to junction defects[7,24–26] ($\sim 1\ \mu m^{-2} GHz^{-1}$), it is most likely that such a small volume of macroscopically lossy material contains no resonant TLS and thus appears dissipationless. This motivates us to introduce a dimensional cutoff and exclude the participation contribution from this near-junction region. We choose to set this cutoff at a distance of 1 μm from the junction, but any choice on the order of 100 nm to 10 μm

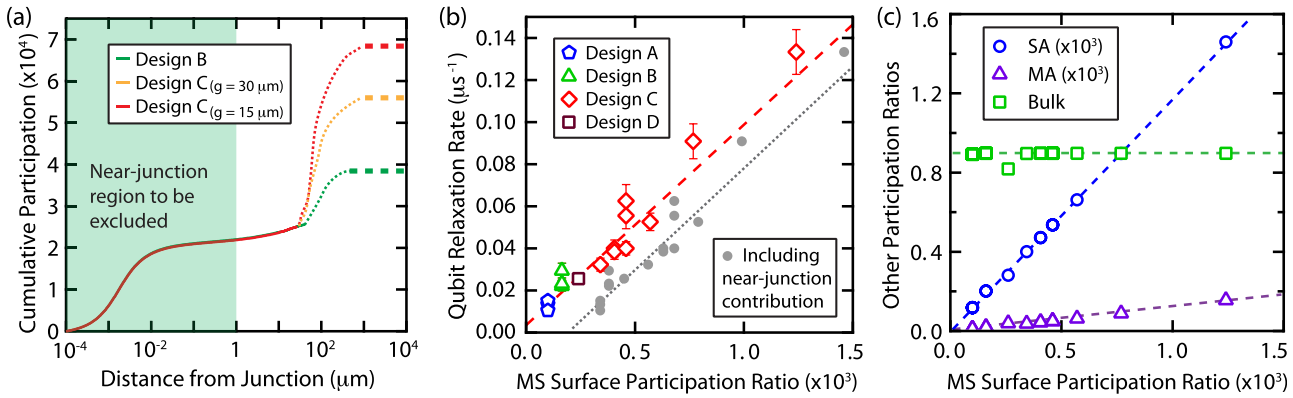

FIG. 3. Surface participation and qubit lifetime. (a) Spatial distribution of simulated surface participation contribution, shown for MS interface of selected transmon designs. Solid curves show cumulative integral of the MS surface participation (p_{MS}) from the electrode leads as they extend from the junction in distance (horizontal axis), indicating total surface participation from the junction to that point. The thick dashed lines indicate the total p_{MS} of all features. The dotted lines notionally represent contribution from the electrode pads as a whole. (b) Open symbols show measured transmon $1/T_1$ as a function of p_{MS} excluding contribution from the sub-micron "near-junction region" (green shaded area in (a)) that most probably contains no TLS. Red dashed line is a fit to Eq. (1). The same set of data including the near-junction contribution is plotted as grey filled circles, with corresponding fit to Eq. (1) shown as the dotted line. (c) SA, MA surfaces, and substrate bulk participation ratios (p_{SA}, p_{MA}, and p_{bulk}) as a function of p_{MS} for transmon devices in this study. Dashed lines are guides to the eye.

does not affect the total participation significantly because the participation contribution from this intermediate region of the electrode leads is insignificant [Fig. 3(a)]. The resultant total p_{MS} from the rest of the MS surface is approximately proportional to the measured $1/T_1$ for all our devices [Fig. 3(b)]. Similarly, we also observe p_{MA} and p_{SA} proportional to $1/T_1$.[22]

The proportionality between qubit decay rate and surface participation ratios strongly suggests surface dielectric loss as the dominant relaxation mechanism for all transmons in this study. Based on Eq. (1), any geometry-independent dissipation mechanism is expected to induce a constant relaxation rate Γ_0 to all our devices. If we were to include the near-junction contribution (as noted above) in p_{MS}, a linear fit of our data to Eq. (1) would produce an unphysical negative y-interception [Fig. 3(b)]. This reinforces the notion of spatial discreteness of surface loss and the necessity of a cutoff. After implementing the cutoff, we see a very small residual qubit decay rate ($3 \pm 1\,\mathrm{ms}^{-1}$), which can be fully explained by the magnitude of quasiparticle dissipation and vortex ac loss as we noted previously. Therefore, there is no evidence of any geometry-independent loss mechanisms, such as from the crystalline substrate or the Josephson junction itself, that limit transmon lifetimes on the level of $Q \sim 10^7$. The absence of loss from the junction may be a result of the small junction size ($0.04\,\mu\mathrm{m}^2$) so that no resonant junction defects are encountered in this study. We also note that surface loss mechanisms consistent with our observed geometric scaling should not be viewed strictly due to impurity or defect-like TLS. Potential alternative mechanisms closely related to surface electric field energy, such as phonon radiation due to surface piezo-electricity,[27,28] may also be broadly included in the surface dielectric loss in this analysis.

We cannot determine which of the three surfaces are the dominant contributors based on these data alone, because all three participation ratios change approximately in proportion when the qubit geometry is varied [Fig. 3(c)]. We can determine a weighted sum of the loss tangents of the three surfaces, $\tan\delta_{MS} + 1.2\tan\delta_{SA} + 0.1\tan\delta_{MA} = (2.6 \pm 0.1) \times 10^{-3}$.

To extend our analysis to distinguish different interfaces, one generally needs to go beyond a planar layout of transmon electrodes, for example, by incorporating striplines or microstrips.

We have further calculated or estimated p_{MS} for reported planar and 3D transmons from the literature,[5,29–37] and Fig. 4 shows the Q factors or T_1's of some of these devices as a function of p_{MS}. All data points with a single-step aluminum lift-off process similar to ours fall near or below the surface-loss line of $\tan\delta = 2.6 \times 10^{-3}$ (red dashed line), consistent with the surface dielectric loss determined in this study. We believe similarly fabricated qubits performing substantially worse

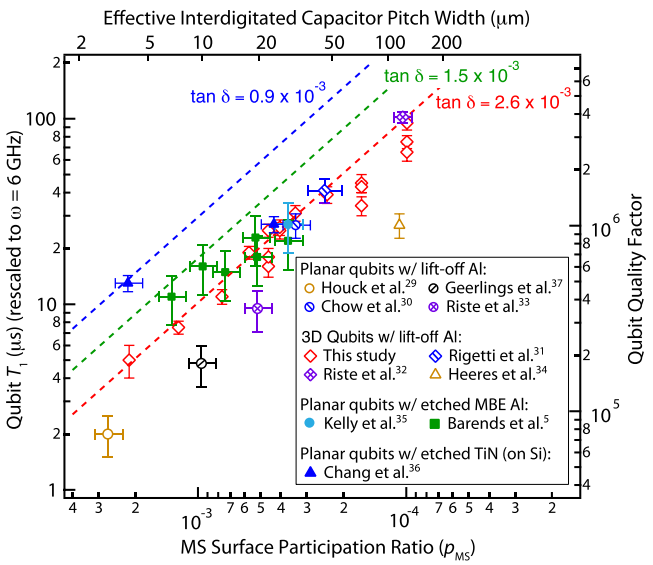

FIG. 4. Transmon lifetime vs. MS surface participation ratio for selected literature data. Open symbols represent various 3D and planar transmons fabricated with the single-step aluminum lift-off process similar to this study. Filled symbols represent transmons with electrode pads fabricated with etch processes to preserve clean MS surface. The vertical axes represent qubit quality factors or the equivalent T_1 at $\omega/2\pi = 6$ GHz. The bottom axis shows p_{MS} in a reversed log scale. The top axis shows the equivalent interdigitated capacitor pitch width of a planar qubit for corresponding p_{MS}, a helpful alternative unit of surface participation.[22]

than this surface-loss line are limited by other mechanisms. Early generation of planar transmons may incur losses due to non-equilibrium quasiparticles or lossy components of the device package,[29] and the 3D "vertical" transmons[34] may be severely limited by conduction loss across the cavity seam.[38]

Several recent studies used subtractively patterned MBE aluminum[5] or TiN[36] films for transmon electrodes. These processes were intended for preserving a pristine MS interface, and subsequent improvement of T_1 suggests the MS interface may indeed play an important role in the total surface loss. We find several data points for these qubits (the leftmost filled symbols) above our $\tan\delta = 2.6 \times 10^{-3}$ line at relatively high p_{MS}, confirming higher surface quality than have been measured in this present study. However, these surface improvements have not been fully translated into the best possible performance for devices with lower p_{MS}, as indicated by their surface-loss bounds (blue and green dashed lines in Fig. 4). It suggests the presence of other dissipation channels yet to be fully suppressed in these high-material-quality planar qubits. These devices also include shadow-mask evaporated junction leads with lower quality surfaces that can have appreciable surface participation and limit qubit T_1.

Looking forward, further advance of coherence times of superconducting qubits will hinge on a combination of improving material surface quality and further reducing surface participation ratios. The state-of-the-art planar transmons have implemented large-sized planar capacitors[30,35] to reduce surface participation, yielding substantial gains in qubit lifetimes. One may naively expect that millimeter-sized 3D transmons may have smaller p_i by orders of magnitude and make dielectric loss irrelevant. The present study shows this is not the case. Furthermore, our simulations find that merely engineering larger and more-separated electrodes will incur significant p_i from the metal leads required to wire up the Josephson junction. Nevertheless, substantial further reduction of surface participation in qubits can be achieved by more complex three-dimensional designs such as deep-etched[39] or suspended structures.[40] With no hard limit in sight, innovative low-participation designs and improved surface quality, together with modest progress in suppressing non-equilibrium quasiparticles, are expected to bring another order of magnitude increase in the lifetime of transmon qubits.

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