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Cite as: AIP Advances **10**, 065120 (2020); https://doi.org/10.1063/1.5138953
Submitted: 15 November 2019 . Accepted: 23 March 2020 . Published Online: 15 June 2020

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ABSTRACT

Nanofabrication techniques for superconducting qubits rely on resist-based masks patterned by electron-beam or optical lithography. We have developed an alternative nanofabrication technique based on free-standing silicon shadow masks fabricated from silicon-on-insulator wafers. These silicon shadow masks not only eliminate organic residues associated with resist-based lithography, but also provide a pathway to better understand and control surface-dielectric losses in superconducting qubits by decoupling mask fabrication from substrate preparation. We have successfully fabricated aluminum 3D transmon superconducting qubits with these shadow masks and found coherence quality factors comparable to those fabricated with standard techniques.

Progress in superconducting circuits for quantum information technologies relies on the improvement of superconducting qubit lifetimes.[1] One of the main sources of energy loss in these devices comes from the dielectric surfaces surrounding the Josephson junctions and associated superconducting circuitry. In particular, a number of experimental results attribute the majority of dielectric loss to one or several of the device–substrate, substrate–air, and device–air interfaces, rather than the bulk dielectrics.[2–11]

State-of-the-art superconducting qubits are fabricated by patterning an organic resist with e-beam or optical lithography to create a liftoff mask, followed by shadow evaporation of the aluminum layer.[12–18] Inevitably, this approach introduces contamination to various interfaces.[5] This includes organic residues from the resist, contamination from the solvents that are required for the resist development after e-beam exposure, and those required for the lift-off process after metal deposition. Furthermore, degassing of the organic mask during metal deposition can lead to additional contamination.

In order to investigate the problems associated with residual contamination and eventually suppress it, we have developed a new nanofabrication technique for superconducting qubits (Fig. 1). Our technique replaces the lift-off of an organic lithography layer with stencil lithography[19] based on free-standing silicon shadow masks fabricated from silicon-on-insulator (SOI) wafers. Consequently, device substrate preparation becomes completely independent from the mask fabrication. As a result, the nanofabrication-related contamination is significantly reduced, and more importantly, controlled studies of surface dielectric losses as a function of surface preparation are now possible. Moreover, the inorganic mask is compatible with high-temperature processes, such as deposition of refractory metals[20] and substrate annealing, which could be performed *in situ*. The silicon mask is free-standing, and thus can be removed from the target substrate at the end of the process and reused for subsequent depositions. It is also tension-free and therefore has higher mechanical stability relative to other possible stencil methods.

The masks were fabricated from 100 mm SOI wafers, which consist of a 500 μm-thick substrate, 200 nm-thick SiO_2 layer, and 5 μm-thick silicon top layer. The wafers incorporate a prefabricated array of 60, (2.7 × 8.6) mm^2, 5 μm-thick, suspended silicon membranes, where the silicon substrate and SiO_2 layer were completely etched away.[21] A schematic cross section of a single suspended silicon membrane is illustrated in Fig. 2(a). The fabrication process starts by creating spacers to control the distance between the mask and the device substrate. The wafer was spin coated at 1000 rpm

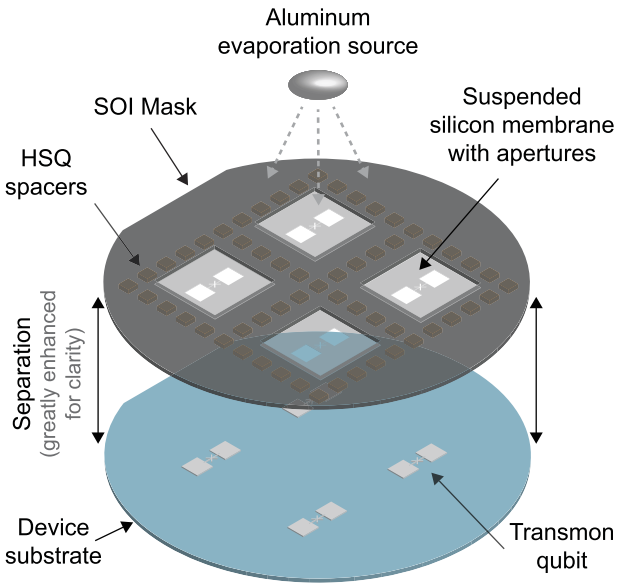

FIG. 1. Concept for nanofabrication of superconducting transmon qubits using free-standing silicon shadow masks (not to scale illustration). A silicon-on-insulator (SOI) wafer incorporates micrometer-thick suspended silicon membranes, which contain apertures with submicron features. The stencil mask is placed on top of another wafer (device substrate). Aluminum is evaporated through it to create transmon structures on the device substrate. The micrometer-size cross-linked HSQ spacers control the distance between the mask and the device substrate. The mask is mechanically separated from the substrate at the end of the aluminum deposition, leaving minimal nanofabrication-related residues. Here, the junction pattern has been caricatured for clarity.

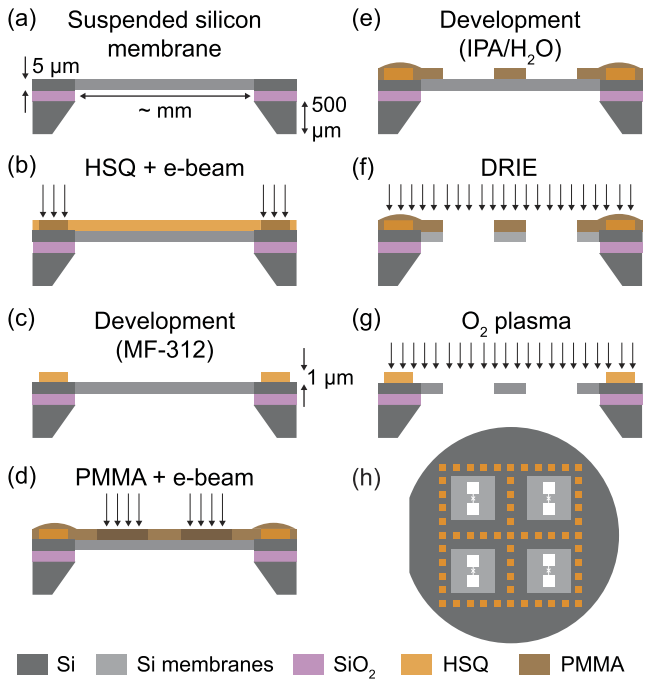

FIG. 2. [(a)–(g)] Schematic cross section diagrams of the free-standing silicon shadow mask nanofabrication process (further described in the main text). (h) Top view schematic of the mask (not to scale).

for 2 min with hydrogen silsesquioxane (HSQ-FOx16), which is a negative inorganic e-beam resist [Fig. 2(b)]. It was then patterned in a Vistec electron-beam pattern generator (EBPG-5000+) with a 100 keV electron beam and developed in MF-312 for 5 min, resulting in arrays of (200 × 200) μm^2 and 1 μm-thick cross-linked HSQ spacers [Figs. 2(c) and 2(h)]. Transmon patterns were defined by apertures in the silicon membranes, created with another step of e-beam lithography. The wafer was spin coated with the PMMA 950 A7 resist at 1500 rpm, baked for 5 min at 200 °C, exposed with a 100 keV electron beam [Fig. 2(d)], and developed in IPA/H_2O (3:1) at 6 °C for 2 min [Fig. 2(e)]. The apertures were created in the suspended silicon membranes by the highly anisotropic deep-reactive-ion-etching (DRIE) BOSCH process[22] [Fig. 2(f)]. As a last step, PMMA and other organic residues were removed from the mask with O_2-plasma cleaning [Fig. 2(g)].

To demonstrate this new nanofabrication method, we focused on a mask design that is suitable for aluminum 3D transmon qubit[14] fabrication. Figure 3 is a simplified schematic describing the metal deposition method. The large rectangular apertures correspond to the capacitor pads and the narrow slits to the leads that will form the Josephson junction of the transmon. The deposition process requires the ability to tilt and rotate the mask-wafer stack with respect to the evaporation source, similarly to that employed in the so-called "Manhattan" process.[23] The first deposition is performed with the stage rotated parallel to the left slit ($\varphi = -45°$) and tilted by angle θ, as shown in Figs. 3(a) and 3(b) and determined by considerations below. By selecting the width of the junction slits to be much smaller than the thickness of the suspended silicon membranes, and selecting θ accordingly, aluminum is deposited through the left slit and lands on the sidewalls of the right slit [Fig. 3(b)]. To accomplish this, the minimum tilt angle should satisfy $|\theta| > \arctan(w/t)$, where w is the width of the slit, and t is the thickness of the silicon membrane. During the first deposition, the two capacitor pads and the first junction lead are formed, as shown in Fig. 3(c). An *in situ* oxidation step is then performed to create the tunnel barrier of the junction. A final (second) aluminum deposition with the stage rotated parallel to the right slit ($\varphi = 45°$) and tilted by θ creates the second junction lead along with another aluminum layer on both capacitor pads [Fig. 3(c)].

Each fabricated mask contains multiple suspended silicon membranes patterned in that way. In Figs. 4(a)–4(c), scanning electron microscopy (SEM) images of a single silicon membrane of a mask are shown. In every membrane, the capacitor pad apertures have dimensions of (530 × 480) μm^2. We designed the width of the junction lead slits such that it gradually reduces in order to minimize possible conductive losses from otherwise long and narrow aluminum leads [Fig. 4(b)]. We vary the minimum width of the junction lead slits w, from approximately 200 nm to 400 nm, in order to create transmons with different junction areas from the same mask. Narrower slits would require further optimization of the DRIE process, as well as thinner silicon membranes.[24] In order to increase the mechanical stability of the suspended silicon structure after etching, we opted to end the lead slits well before their crossing

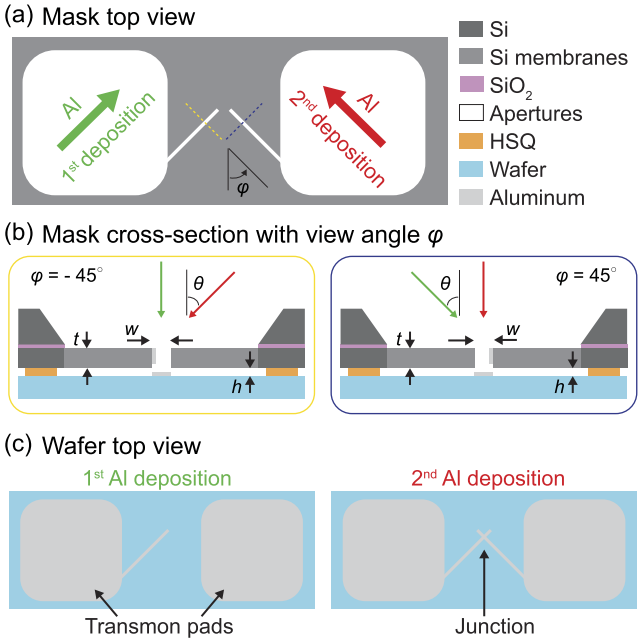

FIG. 3. (a) Simplified mask design schematic. The large apertures correspond to the transmon qubit capacitor pads and the narrow slits to the leads of the Josephson tunnel junction. The green and red arrows indicate the orientation of the Al deposition steps. (b) Schematic cross sectional view (not to scale) of the mask at two distinct positions and angles indicated by the yellow and blue lines. Green and red arrows indicate the tilt angle θ of the first and second deposition steps, respectively. During the first deposition (green arrows), aluminum will only pass through the left narrow slit (yellow cross section), and it will land on the sidewalls of the other aperture (blue cross section). The reverse process occurs during the second deposition step (red arrows). (c) Top view schematic of the aluminum thin-film structure on the device wafer after each deposition step. The first Al deposition creates two capacitor pads and one thin lead, and the second Al deposition creates a second lead and contributes another layer to the capacitor pads. The Josephson junction is formed where these two leads cross.

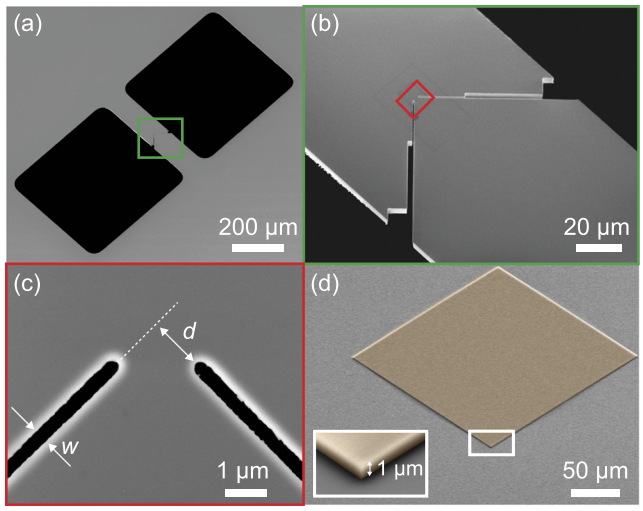

FIG. 4. [(a)–(c)] Scanning electron microscopy (SEM) images of one of the silicon membranes of our free standing silicon shadow mask. Dark areas correspond to apertures and gray areas to suspended silicon. (d) False color SEM image of a 1 μm thick cross-linked HSQ spacer.

point. This imposes an additional condition that the tilt angle satisfies $|\theta| > \arctan(d/h)$ for the two aluminum junction leads to overlap, where h is the mask–substrate separation. The silicon membrane of $t = 5\ \mu$m thickness provides the necessary bending rigidity, which further increases the mechanical stability of the suspended structure. Much thinner silicon would require a modified mask design with in-plane bridges across the slits. In Fig. 4(d), the SEM image of a (200 × 200) μm^2 and 1 μm thick cross-linked HSQ spacer is shown. Arrays of such spacers across the mask are meant to define h and prevent possible adhesion of the mask on the device substrate due to van der Waals forces.

With the mask shown in Fig. 4, we fabricated arrays of 3D transmons[14] on 200 μm-thick, 100 mm diameter c-plane sapphire wafers. The sapphire substrates were cleaned in N-methyl-2-pyrrolidone (NMP) at 90 °C for 10 min, sonicated consecutively in NMP, acetone, and isopropyl alcohol (IPA) for 3 min each, and then dried with nitrogen. All metal deposition and oxidation steps were performed in a Plassys UMS300UHV multichamber electron-beam evaporation system without breaking vacuum in-between steps. After reaching a base pressure less than 5×10^{-9} Torr, we evaporated 21.3 nm aluminum at $\varphi = -45^\circ$ and $\theta = 20^\circ$ at 1 nm/min rate. We then oxidized the aluminum *in situ* with an O_2/Ar (3:17) mixture for 15 min at 100 Torr to create the tunnel barrier of the junction. A second evaporation of 31.9 nm aluminum was done at $\varphi = 45^\circ$ and $\theta = 20^\circ$. A final capping oxidation with an O_2/Ar (3:17) mixture for 5 min at 50 Torr was then performed. The same mask was employed multiple times on different sapphire wafers. The wafers were diced in (8 × 3) mm^2 chips, each containing a single transmon. To do so, we spin coated the wafers with a SC-1827 photoresist layer at 1500 rpm for 2 min and baked it at 90 °C for 9 min. This acts as a protective layer against substrate debris damaging the devices during dicing. The resist was stripped at the end of the dicing process using sequentially NMP, acetone, and IPA. Although the adoption of dicing resist is a convenient practice, it is in conflict here with one of the purposes of our proposed technique, which is to minimize fabrication residues, especially those coming from the organic resist. However, the process of partitioning a wafer into smaller chips is independent of the fabrication of superconducting qubits at the wafer-level, the main focus of our technique. The development of a reliable cleaving technique, which fundamentally does not require protective resist, would be essential for the full elimination of residues on the devices. Nonetheless, acknowledging the above limitation, we tested these devices to determine whether our fabrication technique produces functional transmons.

We characterized six of the fabricated aluminum transmon qubits, coming from two separate sapphire wafers, all corresponding to the mask shown in Fig. 4. In what follows, we present extensive results from one representative device and partial results for the other five. In the optical images of Fig. 5(a), one can identify two aluminum layers that correspond to the two distinct evaporation steps. The double-strip pattern is expected for the double evaporation for a wide slit and does not affect the

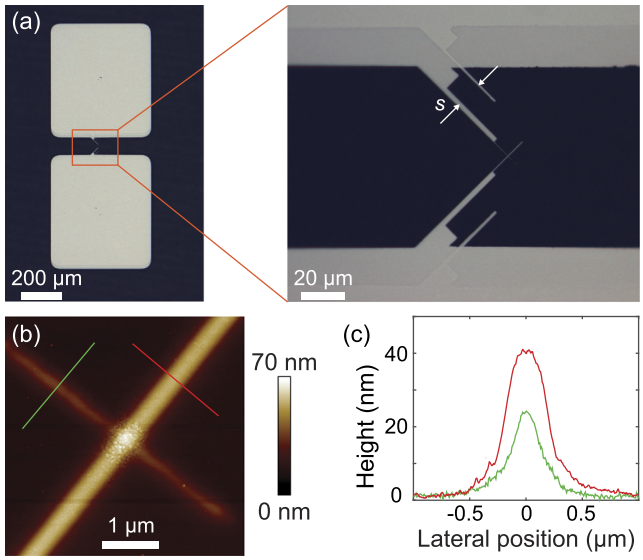

FIG. 5. (a) Optical images of a transmon qubit device fabricated using a free-standing silicon shadow mask. The dark regions correspond to the sapphire substrate and the bright regions to deposited aluminum. (b) Atomic force microscopy (AFM) image of its Josephson junction formed at the crossing point of the two aluminum leads. (c) Height profile for each of the two aluminum leads at the cross sections indicated by green and red color lines in (b).

functionality of the devices. Nonetheless, the distance s between the two strips provides an estimate for the effective mask–substrate separation of $h_{\text{eff}} = s/\tan\theta = 37\ \mu$m. This value is much larger than the thickness of the HSQ spacers (1 μm). We attribute this to built-in residual compressive strain in the silicon device layer of the SOI wafer,[25] which leads to buckling of the silicon membranes upon their release from the Si/SiO_2 substrate. Nevertheless, a notable characteristic of our mask design is that the junction overlap area is approximately independent of the mask–substrate separation, as it is only defined by the width of the two slits. This contrasts with the results of the Dolan bridge technique,[12] in which the junction area depends on both the mask–substrate separation and the width of the slits. We further characterized the device by taking atomic force microscopy (AFM) images of its junction [Fig. 5(b)]. The asymmetry of the widths of the junction leads may be related to misalignment from the intended rotation angle φ, fabrication variances of the mask aperture widths, or more possibly due to different deposition thicknesses for each lead. A characteristic of this technique is that the deposited metallic thin films tend to have larger dimensions than the mask aperture sizes and softer edge profile [Fig. 5(c)], compared to traditional lift-off-based fabrication technologies. This blurring effect can have two distinct origins: the diffusion of the deposited material on the clean, resist-free surface of the substrate, and the geometry of the metal deposition process, which depends on the aluminum source size D, the source–mask separation H, and the mask–substrate separation h.[19,26] The metal deposition setup that was used has a source size of $D = 5$ mm and a source–mask separation of $H = 0.6$ m. For an effective mask–substrate separation of $h_{\text{eff}} = 37\ \mu$m, the enlargement of the feature sizes due to geometrical factors can be estimated to be $w_e = Dh/H = 0.31\ \mu$m. Knowing that the mask aperture widths that were used for this specific transmon were approximately 200 nm, this second effect partly explains the aluminum leads profile of the device [Fig. 5(c)]. However, it cannot be the only feature enlargement effect, since the profile of the sidewalls is less steep than one would expect if the enlargement effect was only due to geometric factors. Therefore, we believe that the resulting soft and elongated cross section profile of the aluminum junction leads [Fig. 5(c)] is a convolution of both diffusion and geometric effects. As blurring can be a limiting factor for smaller junction sizes, further investigation and modeling of the metal deposition dynamics are required. We further characterized the tunnel junction properties of the device, by measuring the normal-state resistance $R_n = 6.9$ kΩ of its tunnel junction, employing two-probe DC measurements, and estimating the critical current to be $I_c = 41$ nA with the Ambegaokar–Baratoff formula $I_c = (\pi\Delta)/(2eR_n)$, where $\Delta = 180\ \mu$eV is the aluminum superconducting gap. This value corresponds to a critical current density of $J_c = 33$ A/cm^2, assuming a junction area of $A_j = 0.12\ \mu$m^2, as extracted from the full-width-half-maximum of the junction lead profiles [Fig. 5(c)]. The average critical current density that we measured for all the devices fabricated with the same mask on the same sapphire substrate is $\bar{J}_c = 42 \pm 10$ A/cm^2. This value is similar to those measured for usual aluminum tunnel junctions that we have fabricated with standard techniques and similar oxidation parameters.

The coherence properties of the transmon qubit, which is shown in Fig. 5, were measured in a dilution refrigerator with a base temperature of approximately 20 mK, adopting a standard circuit quantum electrodynamics (cQED) architecture in the dispersive readout regime.[27] The chip was mounted in an aluminum 3D rectangular-waveguide readout cavity[14] with fundamental mode at frequency $\omega_r/2\pi = 9.1$ GHz (supplementary material). The measurements were performed in reflection and the input/output signals were coupled to the cavity through a single port with coupling rate set at $\kappa/2\pi = 2.5$ MHz. The reflected signal from the readout cavity was amplified by a near quantum limited Josephson array-mode parametric amplifier (JAMPA).[28] The transmon had ground-to-first-excited-state transition frequency $\omega_{ge}/2\pi = 6.01$ GHz, anharmonicity $\alpha/2\pi = \omega_{ge} - \omega_{ef} = 0.23$ GHz, and cross-Kerr to the readout cavity mode $\chi_{qr} = 1.2$ MHz. We characterized its coherence properties by performing interleaved repeated measurements of its T_1 energy relaxation time, T_{2R} Ramsey, and T_{2e} Hahn echo dephasing times for approximately 13 h [Fig. 6]. The length of each measurement was 64 s, 101 s, and 65 s, respectively. We found that the coherence values fluctuate in time with mean values of $\overline{T}_1 \cong 95\ \mu$s, $\overline{T}_{2R} \cong 50\ \mu$s, $\overline{T}_{2e} \cong 85\ \mu$s, and standard deviations of $\sigma_{T_1} \cong 5\ \mu$s, $\sigma_{T_{2R}} \cong 3\ \mu$s, and $\sigma_{T_{2e}} \cong 5\ \mu$s. The measured $\overline{T}_1$ corresponds to a quality factor of $\overline{Q}_{ge} \cong 3.5 \times 10^6$, which is comparable to the state-of-the-art aluminum transmon qubits.[29] Nevertheless, further experimental studies are required to determine whether the energy relaxation properties of this device are limited by surface dielectric losses,[6] nonequilibrium quasiparticle excitations,[29,30] or other loss mechanisms. The fluctuations of T_1 and T_2 as a function of time are similar to what we and other groups[14,29,31] have observed with the same aluminum transmons but fabricated with standard techniques, and can be explained by uncontrolled sources of noise or fluctuating loss channels in the device. The low T_{2R} Ramsey and T_{2e} Hahn echo dephasing times, compared to the $T_2 = 2T_1$ limit, can

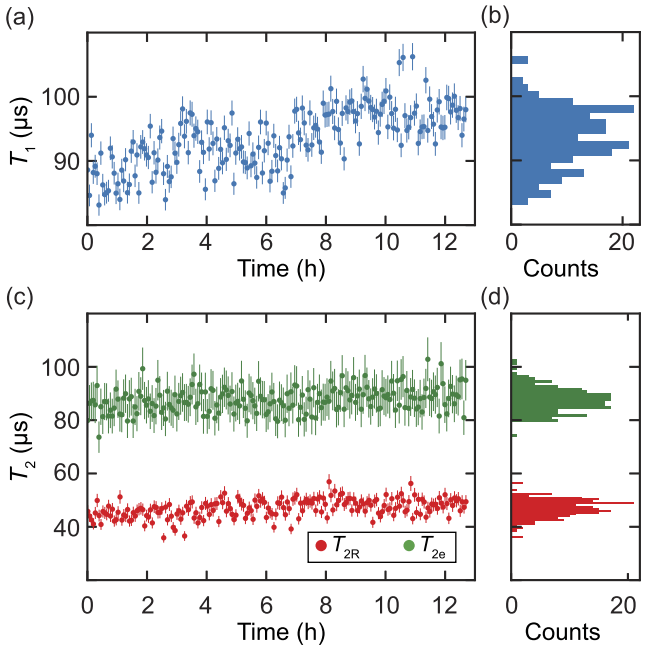

FIG. 6. [(a) and (c)] Fluctuations of the coherence of the transmon qubit, which is shown in Fig. 5, as a function of time. Interleaved measurements of T_1, T_{2R} Ramsey, and T_{2e} Hahn echo times were performed for approximately 13 h, with sampling times of 64 s, 101 s, and 65 s, respectively. The resulting mean measured values were $\overline{T}_1 \cong 95\ \mu s$, $\overline{T}_{2R} \cong 50\ \mu s$, and $\overline{T}_{2e} \cong 85\ \mu s$. [(b) and (d)] Corresponding histograms for the measurements with standard deviations of $\sigma_{T_1} \cong 5\ \mu s$, $\sigma_{T_{2R}} \cong 3\ \mu s$, and $\sigma_{T_{2e}} \cong 5\ \mu s$.

be attributed to the residual thermal photon population in the 3D aluminum readout cavity modes.[32] The reproducibility of the fabrication technique was further assessed with coherence measurements of five more devices, fabricated with the same mask on two separate sapphire wafers. All measurements yielded transmons with energy relaxation times of more than 16 μs. A table with the full properties of all measured transmons that have been fabricated with the presented technique is given in the supplementary material.

Single tunnel junctions have been previously fabricated with free-standing shadow masks based on silicon nitride (Si_3N_4) membranes.[33,34] However, in these efforts, the auxiliary probe-electrodes were fabricated in a separate step in advance. An advantage of free-standing membranes based on silicon, compared to Si_3Ni_4, is that they are nominally free from residual in-plane tensile stress. As a result, silicon masks are mechanically robust enough to implement complex asymmetric aperture designs, allowing for better control of the Josephson junction area independent of the mask–substrate separation. Additionally, large and small features can coexist on the same membrane. This provided us the means to fabricate tunnel junctions and the necessary auxiliary circuitry of a superconducting qubit device, such as the large capacitor pads of a 3D transmon qubit, using a single free-standing mask, reducing fabrication residues on the entire qubit device. Furthermore, our technique eliminates the need to align the tunnel junction with respect to the auxiliary circuitry. Inorganic shadow masks based on the Ge/Nb bilayer have also been used for the fabrication of aluminum tunnel junctions by Welander *et al.*[35] In their work, Ge/Nb thin films are deposited and processed directly on the device substrate, which could potentially introduce additional contamination relative to free-standing inorganic masks.

In conclusion, we have developed a novel nanofabrication technique for superconducting qubits that is based on inorganic free-standing silicon shadow masks, fabricated from SOI wafers. We fabricated aluminum 3D transmon qubits with these masks and performed preliminary observations of their coherence properties. Our work addresses the residual contamination drawbacks inherent to e-beam and optical lithography techniques, providing a solid experimental platform to better understand, control, and potentially minimize surface-dielectric losses in planar superconducting circuits. This technique accomplishes full decoupling of the mask fabrication from device substrate preparation and thus minimizes cross-contamination between the mask and the device substrate. Systematic investigations of the effect of substrate treatment on surface dielectric losses without the restrictions imposed by organic resist processes are made possible. A key advantage of inorganic masks is their ability to sustain high metal deposition temperatures. To this end, free-standing silicon shadow masks hold promise as a suitable technique to fabricate high-quality superconducting qubits based on refractory materials with a larger superconducting gap, such as niobium or tantalum.[20] In addition, high temperature substrate annealing[8] can now be achieved *in situ*, under high vacuum, just before metal deposition, to further improve the surface properties of the device wafer. Finally, this technique is fully compatible with the fabrication of planar superconducting resonators, bringing to these necessary auxiliaries of tunnel junctions all of the aforementioned advantages.

See the supplementary material for more information regarding the cryogenic microwave measurement setup and the full properties of all measured transmon qubits.

We acknowledge insightful discussions with Michael Rooks, Michael Power, Shantanu Mundhada, Chan U Lei, and Andrew Saydjari. The use of the facilities was supported by YINQE and the Yale SEAS cleanroom. This research was supported by the Army Research Office (ARO) under Grant Nos. W911NF-18-1-0212 and W911NF-18-1-0020 and by the Multidisciplinary University Research Initiatives-Office of Naval Research (MURI-ONR) under Grant No. N00014-16-1-2270.

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