Abstract

Resolved dynamics of single electron tunneling using the RF-SET

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This thesis presents measurements of time resolved single electron tunneling events in a metallic thin film circuit. The single electron trap is a circuit consisting of two small metallic islands connected in series with two tunnel junctions and can be fabricated to have tunable microsecond tunneling rates. Capacitively coupling this circuit to the island of a radio frequency single electron transistor, I have time resolved these tunneling events. The trap is operated in a regime where tunneling due to thermal fluctuations is completely suppressed, and tunneling proceeds fluctuations that are purely quantum in nature. I present here the first measurements of the dynamics of these quantum fluctuations, or cotunneling events, with excellent agreement with theoretical predictions, which were developed more than two decades ago. These measurements provide insight into charge fluctuations in nanostructures and demonstrate the possibility to measure higher moments of charge fluctuations in metallic systems.

Resolved dynamics of single electron tunneling using the RF-SET

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List of Symbols and Abbreviations

B	Bandwidth
β	$1/k_BT$
C	Capacitance
C_g	Gate Capacitance
C_j	Tunnel junction Capacitance
C_Σ	Sum Capacitance
e	The charge on the electron, $1.60217653(14) \times 10^{-19}$ C
E	Energy
E_C	Charging Energy
f	Frequency (measured in Hz)
Γ	RF reflection coefficient or Tunneling Rate
g	Dimensionless conductance $g = h/e^2R_j$
h	Plank's Constant
$\hbar$	Plank's Constant divided by 2π
HEMT	High Electron Mobility Transistor
I	Current
n	Number of excess island electrons
n_g	Equivalent gate charge, $n_g = C_gV_g/e$

k_B	Boltzmann constant, $1.3806505(24) \times 10^{-23}$ J/K
κ	Coupling coeficient
ω	Angular frequency (measured in radians per second)
NRAO	National Radio Astronomy Observatory
R	Resistance (measured in Ω)
RF-SET	Radio frequency Single Electron Transistor
R_j	Tunnel junction resistance
R_K	Resistance quantum h/e^2
SEM	Scanning Electron Microscope
SET	Single Electron Transistor
T	Temperature
T_N	Noise Temperature
V	Voltage

Chapter 1

Introduction

Over the past two decades, investigations of single charge devices, where the Coulomb interaction of electrons in nanostructures determine the electron transport, have revealed a wealth of interesting physics and spawned applications in precision measurement, metrology, and detectors. However, nearly all experiments with these systems have probed steady-state time-averaged properties such as the average current flow. More recently, there has been increased interest in noise properties of mesoscopic systems, and it has become clear that the current noise of quantum mesoscopic conductors can provide powerful new insight into the behavior of electrons on the nanoscale. There are numerous experiments on current fluctuations but very few on charge fluctuations. I present in this thesis time resolved single electron tunneling events that allow us to probe the dynamics of charges in nanostructures. These experiments provide a basic test of the theory of cotunneling, or quantum fluctuations. The cotunneling theories were developed two decades ago but the dynamics have never before been tested experimentally.

Early mesoscopic physics experiments focused on transport measurements to study the underlying interactions of electrons. It has more recently been clear that there is much to be learned from studying the fluctuations, or the noise in these systems [Beenakker2003]. For example, current noise has been used to identify the charge of fractionally-charged quasiparticles in the fractional quantum Hall effect [Saminadayar1997, dePicciotto1997, Reznikov1999]. While current noise probes the question of how electrons are partitioned into reflected and transmitted beams by a phase coherent scattering region, charge noise probes the issue of how long electrons spend in the scattering region. Insights revealed studying charge noise may prove to be as powerful as those derived from studying current fluctuations. Also, for typical mesoscopic detectors such as the single electron transistor and

the quantum point contact, it is the charge fluctuations which are responsible for the backaction, or the unavoidable disturbance of the measured system caused by the detector. Detailed measurements of charge fluctuations can serve as probe for measuring the backaction of the detector, the knowledge of which will aid in the design of more efficient quantum detectors and amplifiers.

In single electron systems, such as the single electron transistor or the quantum point contact, transport can be strongly affected by small changes in potential or by the motion of individual charges nearby. The current through these devices flows via tunneling between a small number of single-particle or single-charge states, but there are very few experiments in which the dynamics of the tunneling of single charges have been directly observed. There are two main reasons for this, and both are related to the smallness of the electron's charge, e. First, the typical rates of tunneling are very fast (MHz to GHz or higher), since they are limited by the size of a measurable current (f=I/e = 6.24 MHz/pA) or by the timescale of thermal fluctuations (kT/h = 1 GHz at 50 mK). Second, the signal created by motion of a single electron is very small. This thesis works to overcome these obstacles by working at the problem from both sides. First, I make use of the radio frequency single electron transistor (RF-SET) developed by Robert Schoelkopf [Schoelkopf1998], which possesses single-electron sensitivity and 100 MHz of bandwidth. Secondly, I have fabricated circuits that can slow the electron tunneling rates down into a measurable range. The combined effect of the fast electrometer and the circuit with relatively slow tunneling events is that single tunneling events can be resolved in the time domain. More specifically, I have been able to directly resolve the cotunneling, or quantum fluctuations, in a single electron circuit. This serves as a basic test of our understanding of cotunneling theory in a single electron trap, which will aid in improving the performance of single electron pumps and turnstiles.

1.1 Charge Detection with the RF-SET

The single electron transistor, shown in Figure 3.1, consists of two small ($50 \times 50\ nm^2$) tunnel junctions in series with a small island between them. A typical charging energy for this circuit is in the range of 1-2.5 K, and at sufficiently low temperatures ($\sim$ 50 mK), no current can flow between the drain and the source. This is known as Coulomb blockade and is extremely sensitive to the potential of the island. If the correct voltage is applied to a nearby gate $Q_g = C_g V_g = e/2$, this blockade can be lifted, allowing current to flow, switching on the transistor. The potential of the SET island is periodic in this gate with a period of one electron. It is also sensitive to any nearby

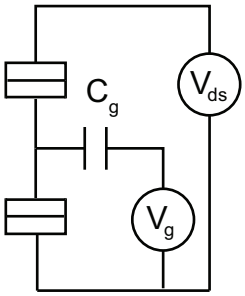

Figure 1.1: Circuit diagram for the single electron transistor, consisting of two tunnel junctions in series with a small metallic island between them. The potential of the island is tuned with the nearby gate.

gate, so in addition to the intentional gate, we can couple another single electron device, such as the single electron box.

The SET was first proposed in 1986 by Averin and Likharev [AVERIN1986], and was first measured at Bell Laboratories in 1987 by Fulton and Dolan [FULTON1987]. Measurements of the drain-source current flow through the SET enable high precision charge measurements of nearby devices. The SET is capable of detecting signals much smaller than a single electron. These devices have quite high resistances ($> 26\ k\Omega$), however, so long RC times limit these measurements to ∼kHz ranges. Despite the limitations of bandwidth and sensitivity of these DC-SETs, they have been used to measure macroscopic charge quantization [LAFARGE1991], characterize and operate single electron pumps and traps [Keller1996, DRESSELHAUS1994], and to measure the local chemical potential in semiconductor systems [Wei1997, Yoo1997].

Improvements to the bandwidth and sensitivity of the SET were made with the invention of the RF-SET [Schoelkopf1998], which utilizes a measurement technique in which the SET is embedded in an LC resonant circuit. This not only increases the measurement bandwidth to >100 MHz, but also moves the measurements away from the ubiquitous low frequency 1/f noise. The best charge noise obtained with the RF-SET is about $5 \times 10^{-6} e/Hz$, only a factor 3 greater than the theoretical limit [Devoret2000].

The RF-SET has both the speed and sensitivity required for rapid electron counting measurements. The particular RF-SET used in the main section of this thesis has a charge sensitivity of $7 \times 10^{-5}\ e/Hz$. The signal size on the SET comes from the amount of polarization charge caused by a change in one electron on the measured circuit, for example, a single electron box. The figure of merit is the dimensionless coupling ratio $\kappa = C_c/C_\Sigma$, where C_c is the coupling capacitance and C_Σ

is the sum capacitance of the measured island. Given a coupling of 10%, the maximum rate that electrons can be time resolved with the RF-SET with a single to noise ratio of 1 is greater than 1 MHz.

1.2 Measurements of Average Charge

Using the circuit shown in Figure 1.2, where a single electron transistor is used as an electrometer, measurements of the *average* charge state of a small metallic island, in the single electron box, can be performed with exquisite precision. The box is the simplest single electron circuit [LAFARGE1991], consisting of a single island connected to a reservoir through a small capacitance tunnel junction. A voltage on a capacitively coupled gate allows adjustment of the electrochemical potential of the

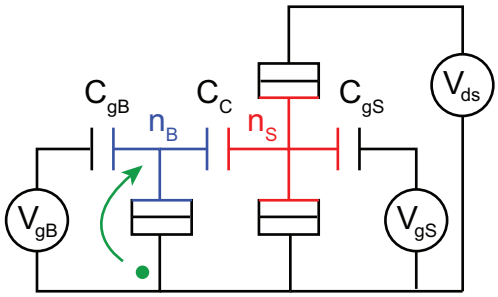

Figure 1.2: Circuit diagram showing the single electron transistor capacitively coupled to the single electron box. The size of the signal on the SET is determined by the coupling capacitor C_c, which sets the amount of polarization charge is induced on the SET due to a change in one electron on the box.

island. The electrostatic energy of the box, $E = E_C(n_{gb} - n)^2$, depends on the number of excess electrons on the island, n, and the applied gate, expressed as an effective gate charge, $n_{gb} = C_{gb}V_{gb}/e$. The energy scale of this circuit is the charging energy of the box, $E_c = e^2/2C_{box}$ (typically 1-2 K), where C_{box} is the sum capacitance of the box island. The electrostatic energy is plotted as a function of gate charge for different charge states in Figure 1.3a, and consists of a series of parabolas which cross at charge degeneracy points where n_{gb} takes on half integer values. In the absence of thermal or quantum fluctuations, the charge state should then change in a step-wise fashion shown in Figure 1.3b at these degeneracy points, and a measurement of the average charge $< n >$ will display the Coulomb staircase [LAFARGE1991]. At finite temperature, there can be a thermal occupation of higher energy charge states, which leads to a thermal broadening of the transitions in the staircase.

The first measurements of the Coulomb staircase using the RF-SET were performed in our

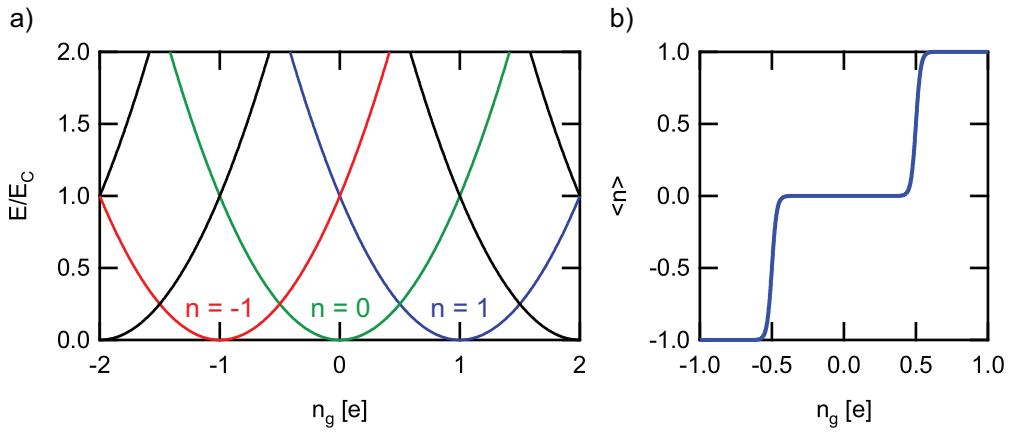

Figure 1.3: a) Energy level diagram for the single electron box. The Coulomb energies for several values of the charge state on the box, n, are plotted as a function of applied gate charge. The points at which these curves cross are the charge degeneracy points. b) The average charge on the box is plotted as a function of trap gate for a box with charging energy $E_c = 1.5\ K$ at 50 mK. This is known as the Coulomb staircase of the single electron box. The charge on the box increments by one at each of the charge degeneracy points.

group [Lehnert2003]. Using the high sensitivity of the RF-SET and an integration time of several seconds per point, the staircase as a function of gate voltage, temperature, and magnetic field was measured to a precision of about a part in 1,000, about two orders of magnitude improvement over measurements [LAFARGE1991] with a conventional SET. These measurements revealed that the broadening and the detailed shape of the staircase were distinctly different from that predicted by a simple model of thermal activation to higher charge states. The presence of the tunnel junction coupling the island to the reservoir, which allows the charge state to change, also couples the charge states to quasiparticle excitations in the Fermi seas of the reservoir and island themselves. This coupling means that even at zero temperature, there can be quantum fluctuations of the charge state of the island, leading to a rounding of the staircase and a logarithmic renormalization of the charging energy. These were the first measurements of this physics in the single electron box and there was excellent agreement with theory with no adjustable parameters as shown in Figure 1.4. A significant body of theoretical work [Goppert2001] has addressed this problem for the single electron box. What makes this different from what has been done in quantum dots is that there are many conduction channels in a metallic junction, each with small transparency, but combining to give a conductance comparable to the quantum conductance. Also, the single-particle level spacing in these metallic islands is negligibly small.

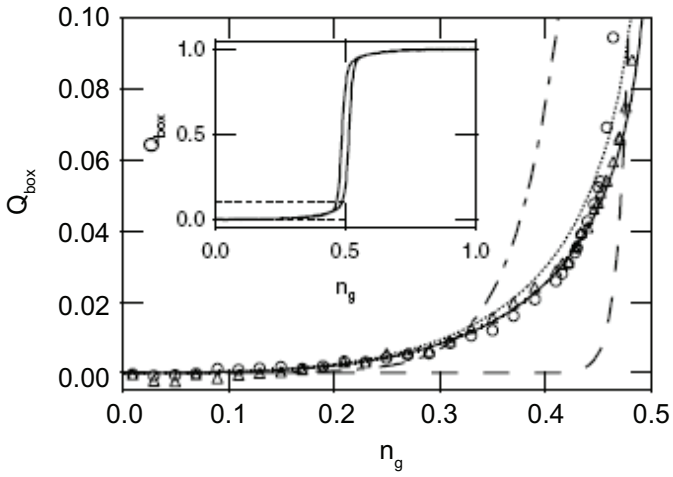

Figure 1.4: Precision measurement of the Coulomb staircase of the single electron box (adapted from Lehnert et al. [Lehnert2003]. The average charge on the box as a function of gate charge is shown for one step of the box near charge degeneracy. The data is measured at two different bias points of the SET. The dashed lines show thermal broadening of the staircase at 30 mK and 125 mK, and the solid lines shows the theoretical prediction for the quantum charge fluctuations [Goppert2001] with no adjustable parameters.

These measurements revealed some non-trivial effects of charge fluctuations in mesoscopic metallic systems, but there is still no information about the actual dynamics of the island charge state, since the SET is measuring the ensemble averaged charge state on timescales of seconds. Other work in our group has used the RF-SET to measure the Cooper-pair box, which acts as a coherent two level system. The RF-SET was used to temporally resolve the relaxation of the charge state (still an ensemble average over thousands of repetitions, however) on sub-microsecond timescales, and to measure the relaxation time (T1) of these solid state qubits [Lehnert2003a]. The actual dynamics for the single electron box, however, are typically much faster (ns), and take place in a random, Poisson distributed manner, making it very difficult to time resolve single electron tunneling events.

At low temperatures, we can consider the dynamics between the two lowest charge states of the box. If we were able to time resolve the charge on the box island, we would observe random telegraph noise with the charge fluctuating in a Poisson-distributed manner between the two charge states. At $n_{gb} = 0$, the box spends almost all of its time in the $n = 0$ state with rare excursions into the $n = 1$ state. At this point, the tunneling rate $\Gamma_{0\to1}$ is negligibly small, but this causes $\Gamma_{1\to0}$ to be extremely high. An illustration of this is shown in Figure 1.5. Here, the downward tunneling rate is of order gE_C/h (typically 10 GHz or more), where g is the dimensionless conductance of the junction

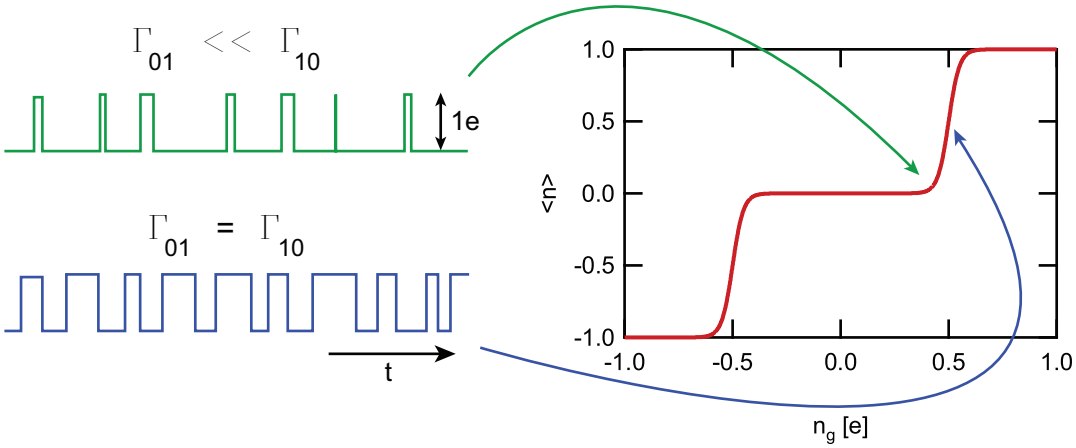

Figure 1.5: Illustration of the charge fluctuations in the single electron box. At low temperatures, only the two lowest energy levels need to be considered. A time resolved measurement of the charge on the box would reveal random telegraph noise as shown in the two figures on the right. Away from charge degeneracy, one rate can always be made small. For example, as shown in the upper green curve, $\Gamma_{0\to1} << \Gamma_{1\to0}$, but this comes at the cost of one rate that is very large resulting in series of near delta-functions in the time record. The best point to measure is near charge degeneracy, shown in the lower time record. For a metallic box, however, rates here are still $\sim$1 GHz

and is of order 0.1-1. The best case scenario for detection, would be at the charge degeneracy point, where the box spends an equal amount of time in each state. Even here, however, the rates are still of order gk_BT/h, which is about 1 GHz for a dimensionless conductance of 1 and a temperature of 50 mK. This makes measurements of time resolved tunneling events in a metallic box with an RF-SET technically infeasible. Such measurements have been performed with a semiconductor quantum dot [Lu2003, Fujisawa2004, Gustavsson2006, Fujisawa2006], where a gate can be used to pinch off tunnel coupling between the dot and reservoir in-situ, making the rates of sequential tunneling measurable ($<$ 1 MHz).

The fast tunneling events in the single electron box were appreciated early on. Since the dimensionless conductances in a metallic junction can only be fabricated reliably in a narrow range of $0.01 - 1$, the solution to slowing down the tunneling rates has been to add several junctions in series.

1.3 Charge Dynamics

In multi-junction single electron systems such as the single electron trap and the single electron pump, tunneling rates are greatly reduced by putting many tunnel junctions in series. Charges

are transferred into an intermediate state with a large Coulomb energy cost, leading to a strong suppression of the sequential tunneling rates. The dynamics should then be dominated by rates of virtual tunneling via the forbidden intermediate states, a process known as cotunneling [Averin1992].

The single electron pump is a device that uses multiple junctions to suppress sequential tunneling. Shown in Figure 1.6a, the pump consists of an island connected to a reservoir, as in the electron box, but in this case, this connection is via a series of several small capacitance islands and junctions. By

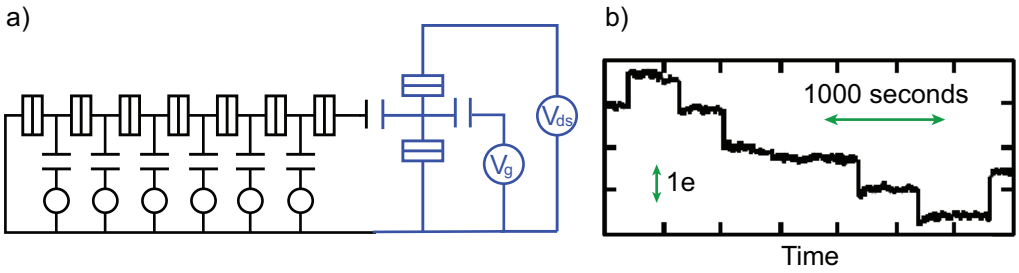

Figure 1.6: The single electron pump. a) Schematic of the seven-junction electron pump, with an SET electrometer which measures the last island. The six islands are biased in a sequential fashion to pump charge on and off the island. b) Measurement of single electron changes in the pump's charge state, in the "hold mode" where the gates are fixed (adapted from Keller et al. [Keller1996]). Very rare jumps of size 1e are observed on timescales of minutes to hours, representing "errors" in the pump due to high order tunneling processes. The error rates and their mechanism are not fully understood.

pulsing the gates of the intervening islands in a sequential manner, an electron can be transferred in a "bucket-brigade" fashion, and pumped from reservoir to island. The pump is a very successful device which can transfer electrons (in its seven-junction implementation) with an absolute accuracy [Keller1996] of about 10 parts per billion, and is being adopted as a new quantum standard for capacitance [Keller1999].

The pump can be placed in "hold" mode, where an electron is transferred to the end island and the gates are held fixed. The pump is then operated as an electron trap, and the lifetime of the charge on the island can be measured, as shown in Figure 1.6b, by measuring the island's charge with a conventional dc SET. Individual tunneling events take place randomly, on a timescale of seconds to hours, which is required for these slow charge measurements. Similar experiments observing very slow tunneling events in multi-junction traps were also performed by earlier groups at Stonybrook [DRESSELHAUS1994] and Saclay [LAFARGE1992].

The dynamics of these multi-junction devices are not fully understood. The error rate of the five

junction pump was deemed sufficient for operation at metrological accuracy for the capacitance standard, but the measured rates disagreed with those due to sequential and cotunneling events predicted by theory by 17 orders of magnitude during operation in "hold" mode [Kautz2000]. Metrological accuracy was attained only after increasing the number of junctions to seven. The measured error rates in this setup were extremely small, but still disagreed with theoretical predictions by several orders of magnitude. The errors in the pump were attributed to photon-assisted tunneling, and the tunneling rates are due to sequential, single-junction tunneling [Kautz2000]. These dynamical studies of metallic junctions do not shed much light on the problem of mesoscopic charge noise, nor do they provide a direct test of cotunneling.

Recently, the first experiments observing single tunneling events in simple semiconductor quantum dots using high speed electrometers have been performed. Rimberg and co-workers at Rice University [Lu2003] integrated a metallic RF-SET on top of a semiconductor dot, and were able to resolve sequential tunneling events due to thermal activation, by pinching off the tunnel coupling of the island to the reservoir, reducing g and therefore the tunneling rate. Fujisawa and coworkers at NTT [Fujisawa2004] used two semiconductor SETs, the first configured as an RF-SET electrometer, to measure the single thermal tunneling events in the second SET, and to observe the speed-up of tunneling due to a current passed through its drain and source. Quasiparticle tunneling rates onto the island of an SET were measured by Naaman and Aumentado at NIST [Naaman2006a]. These are impressive technical demonstrations that the RF-SET can indeed measure single charge tunneling events at MHz rates. These results show the technical possibility of probing single-electron dynamics, but do not yet offer much new information about the physics of single charge devices. Also, the processes in all of these cases being studied are only that of ordinary sequential tunneling.

A recent experiment by Per Delsing and co-workers at Chalmers University [Bylander2005] has used an RF-SET to observe the correlation of tunneling events in a long 1-dimensional array of metallic junctions. In such arrays, charges are predicted to move as interacting solitons, leading to a moderate correlation of electron tunneling times, which were sensed by a direct (rather than capacitive) connection to the measuring island of an RF-SET. This correlation leads to a noise spectrum with a peak at frequency $f = I/e$, observed in the output of the RF-SET. This result demonstrates the kinds of non-trivial physics, due here to electron-electron interactions, which a dynamical measurement can reveal.

1.4 Electron Counting with the Single Electron Trap

In the experiments performed for this thesis I used an RF-SET to look at more rapid, intrinsic tunneling dynamics in a two junction trap, a device that is far simpler to operate than the multi-junction traps and pumps. This device has the possibility for reduced tunneling rates from those seen in the single electron box, but still has measurable microsecond time scale dynamics which in this case are dominated by quantum fluctuations. Because I am able to detect tunneling events much more rapidly than was possible with the dc SET in the case of the traps and pumps, rare, anomalous events are relatively unimportant and the statistics are vastly improved. The calculations are also much less complicated for the trap as compared with the pump because of the reduced number of islands. Four charge states of the trap must be considered at low temperature to understand the tunneling rates, while 254 configurations must be considered to calculate the tunneling rates in the 7-junction pump [Kautz2000].

The single electron trap, shown in Figure 1.7a, consists of an intermediate island with charge state n_{Isl} and the trap island with charge state n_{Trap}, and has two separate voltages which bias these islands with gate charges $n_{gi} = C_g V_{gi}$. An RF-SET is connected capacitively to the second island, to measure the charge state on microsecond timescales. As shown in the energy level diagram in Figure 1.7b, and the charge configuration picture in Figure 1.7c, in order to change the charge state of the trap from $(n_{Isl}, n_{Trap}) = (0,0) \rightarrow (0,1)$, charge transfer must proceed via tunneling first to an intermediate state $(1,0)$ of the first island that has a high Coulomb energy. Another possibility is to tunnel through the second junction first $(n_{Isl}, n_{Trap}) = (0,0) \rightarrow (-1,1) \rightarrow (0,1)$. For temperatures less than the charging energies of both islands, $kT < E_{CTrap}, E_{CIsl}$, one need only consider these four states (two for each island) to understand the transport. Charge fluctuations of an electron on and off the trap see this large energy barrier for at least one of the two tunneling steps, so that transport is *uphill both ways*. This greatly reduces the sequential tunneling rates to negligible levels at low temperatures. Tunneling proceeds via a virtual occupation of this intermediate state, which is a purely quantum process. The rates for this process are in the kHz range over a wide range of trap gate voltages and temperatures and are easily resolved using the RF-SET.

The trap circuit is relatively simple compared to the long arrays of junctions in the other experiments measuring dynamics in metallic system, which allows for an easier characterization of the gate voltages. We can map out the full parameter space of this circuit as a function of the gate controls

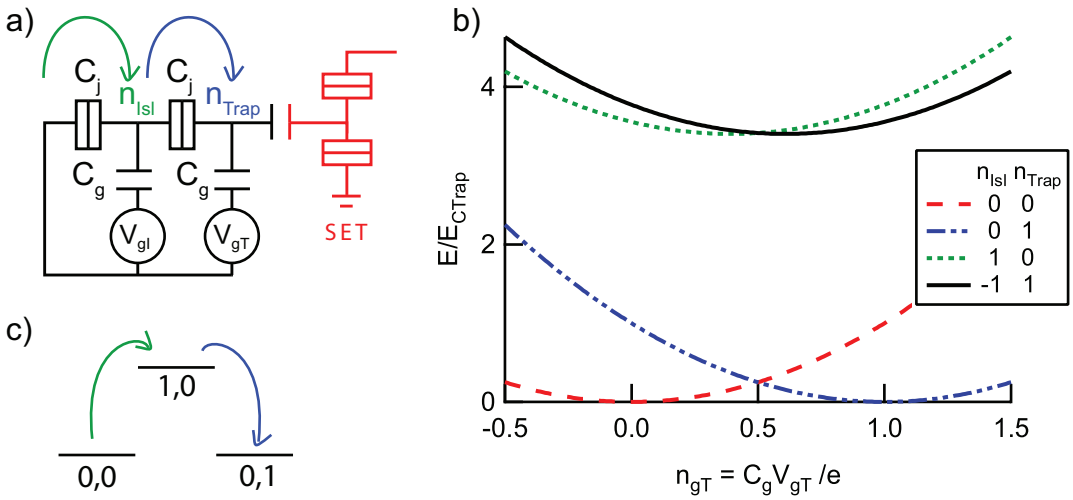

Figure 1.7: a) Circuit diagram of the single electron trap capacitively coupled to a single electron transistor (red). The trap circuit consists of two junctions in series with two islands. The potential of each island can be tuned with capacitively coupled gate voltages V_{gi}. The gates apply an effective charge to the islands, written in terms of the number of applied electrons, $n_i = C_{gi}V_{gi}/e$. b) Energy level diagram showing the four lowest charge states for the trap near the trap energy degeneracy point $n_{gT} = 1/2$. In order to change the charge state on the trap from (0,0) to (0,1), electrons first must tunnel to an an intermediate state with a high Coulomb energy, (1,0) or (-1,1). c) The charge configuration space picture of the trap. This diagram highlights the fact that the electrons must go up hill both ways tunneling on or off of the trap island.

and are able to precisely bias the circuit within this space for measurements of both the statics or time averaged properties as well as the dynamics. The parameter space is mapped out with measurements such as the Coulomb staircase and the hexagonal stability diagram of the trap, as shown in Figure 1.8. We measure the dynamics of the circuit in several different ways, including swept averaged measurements, as shown in Figure 1.8, pulsed gate measurements to observe the relaxation time of electrons on and off the trap island, or we can fix the bias on both gates while making time resolved measurements of the charge with the RF-SET as shown in Figure 1.9. The theory used for predicting the rates of sequential and cotunneling was developed about two decades ago, but there have been few direct measurements of the individual rates for in simple circuits, and no experiments have accessed the mesoscopic charge fluctuations associated with cotunneling. Most experiments have instead probed the current passed through single electron transistors [GEERLIGS1990]. This work presents measurements of the dynamics of the cotunneling rate in the single electron trap and comparisons to these theoretical predictions.

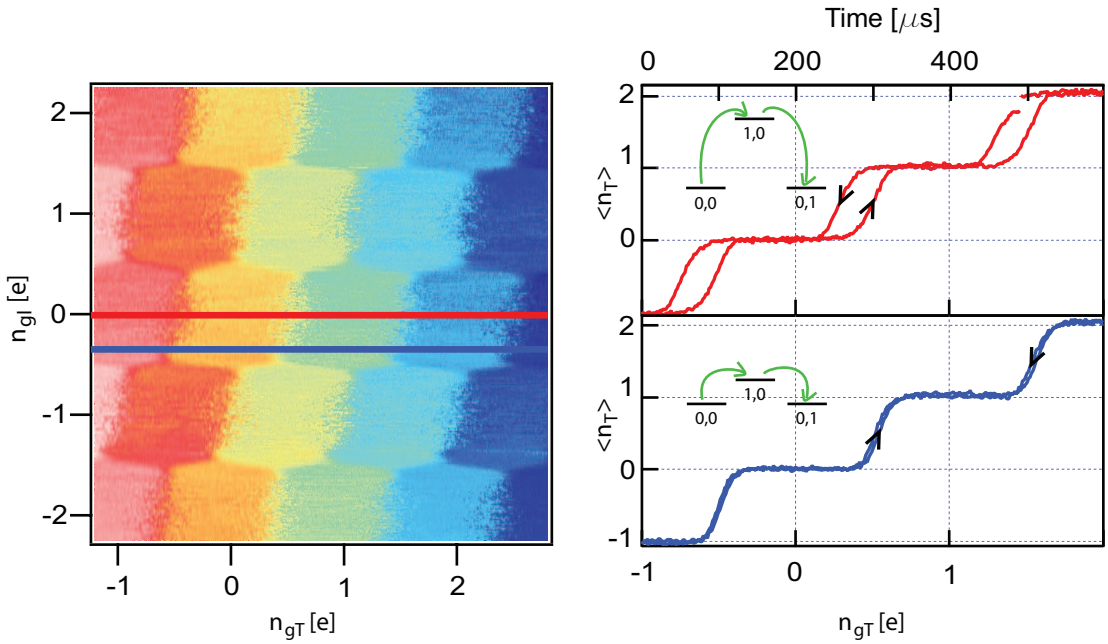

Figure 1.8: The hexagonal stability diagram for the trap is shown on the left. The color blocks represent the ground state of the trap. The lines separating the color blocks indicate a change in the charge state of one of the two islands. The right figure shows the tunability of the tunneling rates. In the top curve, the trap island is maximally blockaded and the rates are low. When the trap gate is swept faster than the characteristic rate, the Coulomb staircase measurement is hysteretic. The lower curve is measured at a bias point where the rates are fast, and for the same trap gate sweep rate, no hysteresis is observed.

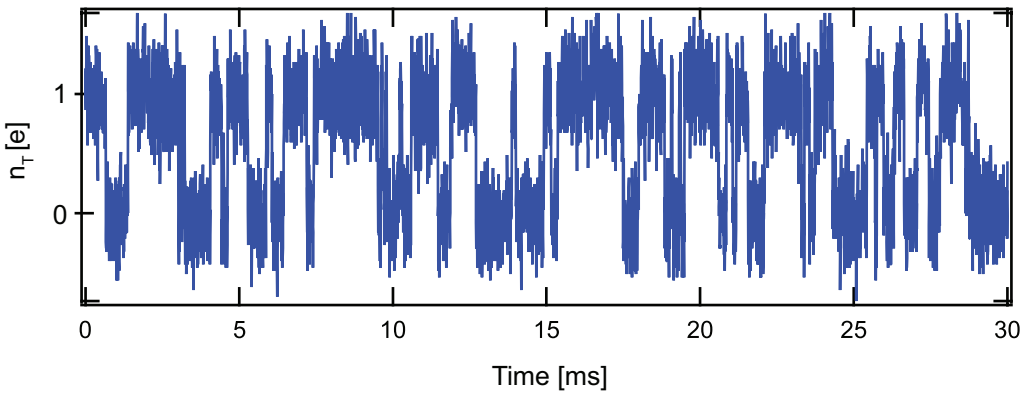

Figure 1.9: Time resolved measurements of trap charge as a function of time.

1.5 Overview of the Thesis

The work done for this thesis contains the entire process for the experiment, from experiment and circuit design, theoretical predictions, electronics and cryogenics, fabrication, and finally measurements. Chapters 2 provides an introduction to single electron circuits, focusing in detail on the single electron box and trap. Chapter 3 continues this discussion to the SET, describing how it is used as an electrometer. This chapter includes a detailed example of how we use the SET to measure charge on a single electron box and how this circuit is used to make high speed measurements. These chapters provide the framework with which we can start to develop an understanding of the dynamics of these circuits.

The dynamics are the focus of chapters 4 and 5. Chapter 4 focuses on the sequential tunneling model, also known as orthodox theory or the global rule. This is the regime in which most experiments operate and where other measurements of dynamics in single electron circuits have been performed. I will show in this chapter that the predicted rates using this model are unrealistically low for the single electron trap. This will then take us to chapter 5 which explores the quantum fluctuations in the trap. These quantum fluctuations are higher order tunneling events that involve cotunneling, or simultaneous tunneling of two electrons. This is a purely quantum process as it proceeds through virtual occupation of a higher energy intermediate state. In this chapter, we will set up the theoretical predictions for the tunneling rates and analyze the feasibility of the measurements.

Careful circuit design is required to achieve the circuits for which the predicted rates are at a measurable level. Chapter 6 discusses the design and realization of circuits that meet these requirements. Simulations for capacitance design will be discussed as well as the electron beam lithography process used to fabricate aluminum thin film circuits with tunnel junctions. Chapter 7 introduces the experimental methods including the setup, cryogenics, and RF circuit design. Measurements to characterize the RF-SET will be presented here.

The main results for this thesis will be presented in Chapter 8. Here I will present measurements characterizing two trap samples. Then, I will go on to discuss the dynamics in these circuits, measured in a variety of ways, including time resolved measurements of single tunneling events. I will show comparisons with the theoretical predictions from chapters 4 and 5 as well as a discussion of the effects of the backaction of the SET. Chapter 9 will present possibilities for future work and concluding remarks.

Chapter 2

Single Electron Circuits

Detection of single tunneling events is difficult for a variety of reasons, mostly having to do with the smallness of the charge of the electron. For even quite small currents, the rates are extremely fast. Taking a naive view of electrical current as individual electrons flowing through a wire, the flow rate is 6.24 MHz/pA. High energy physics experiments involve beams of discrete particles, but in conductors, electrons exist as a quantum fluid of charge and are completely delocalized. The simplest example of this is charging a capacitor with a voltage source. The capacitor acquires a charge $Q = CV$, which depends only on the applied voltage and the capacitance. The charge on the capacitor plates takes on continuous values as the voltage source can be tuned in arbitrarily small increments. More sophisticated techniques are required in mesoscopic systems to break up this fluid into discrete droplets of charge one electron. The requirement is that we have a single electron device. A second difficulty is the small signal size ($1.6 \times 10^{-19} C$) of one electron which necessitates an ultra-sensitive detector. We will exploit the charge sensitivity of a RF-SET of $7 \times 10^{-5} e/\sqrt{Hz}$. Because the signals for even small currents are quite fast, we work at this problem from both sides. First we use the fastest, most sensitive electrometer. Second, we slow the currents down to be in the detectable range of the RF-SET. We also want to be able to compare measurements with theoretical predictions, so we limit the complexity of the design, looking for the simplest circuit that meets these requirements.

A single electron device is a circuit that manifests charge quantization, or "notices" when an additional electron is added or removed. To break up the fluid into discrete droplets of charge, a section of the circuit needs to be separated from the long metallic leads. This is done by fabricating small ($100\ nm\ \times\ 1\mu m$) metallic islands. Second, there must be a way to add or remove charge

from the area in question. If this is not the case, then the charge on the island is always just the continuous polarization charge from neighboring voltage sources which are capacitively coupled to the island. This is done in metallic systems with tunnel junctions, which are comprised of two layers of metal separated by a thin insulating layer, in our case Al:AlO_x:Al. The total capacitance, C, of the island can be small enough so that the energy required to add an additional electron to the island, e^2/C, is large compared with the temperature of the system. The junction itself should be thought of as a capacitor with a finite number of conduction channels. If the junction separating the island from the leads has a resistance much larger than the resistance quantum $R_K = h/e^2$, then the wavefunction of the electron will be localized to the island. When these two conditions together are met, the charge on the island is a good quantum number and takes on integer values n [MATVEEV1991, Devoret1992, Grabert1992].

This chapter will review the single electron box, which is a building block of more complex single electron circuits. Many experiments in mesoscopic physics and quantum computation are based on the single electron box. From there, we will analyze more complicated single electron circuits such as the single electron transistor and the single electron trap. This chapter focuses on the box and the trap, and the next chapter will cover the single electron transistor. This will provide the tools with which we can study the statics and then the dynamics of the electrons in these systems.

2.1 The Single Electron Box

The simplest single electron circuit is the single electron box, shown in Figure 2.1, consisting of a small metallic island connected to a gate voltage through a capacitor and to ground through a tunnel junction. The box is characterized by the charging energy which is defined to be the energy required to add one excess electron to the island, $E_C = \frac{e^2}{2C_\Sigma}$, where C_Σ is the sum capacitance of the island[1]. In the single electron box, this is just the sum of the gate capacitor and the junction capacitance, $C_j + C_g$. A typical single electron box could have a charging energy in the range of 1-3K whereas 30 mK is a temperature easily reached in a dilution refrigerator.

The total electrostatic energy of the circuit is the sum of the energy from the discrete charge states plus the energy added by the voltage supply through the gate capacitor

$$E = E_C(n - n_g)^2 \tag{2.1}$$

[1]Charging energies will be written in terms of equivalent temperatures, for example $E_C = 1\ K$ is used only as a shorthand for $E_C/k_B = 1\ K$.

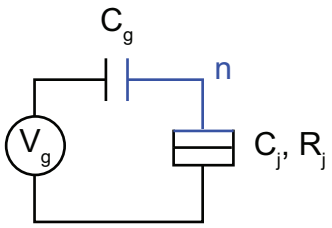

Figure 2.1: Circuit diagram for the single electron box. The box consists of a metallic island coupled to a reservoir through a tunnel junction with capacitance C_j and resistance R_j. The total electrostatic energy of the box is determined by the integer number of excess electrons on the box island, n, and the continuous applied gate charge $n_g = C_g V_g/e$.

where n_g is the polarization charge added through the gate capacitor, $n_g = C_g V_g/e$. The energy level diagram is shown in Figure 2.2. The discrete charge states, n, give energy levels which are a series of

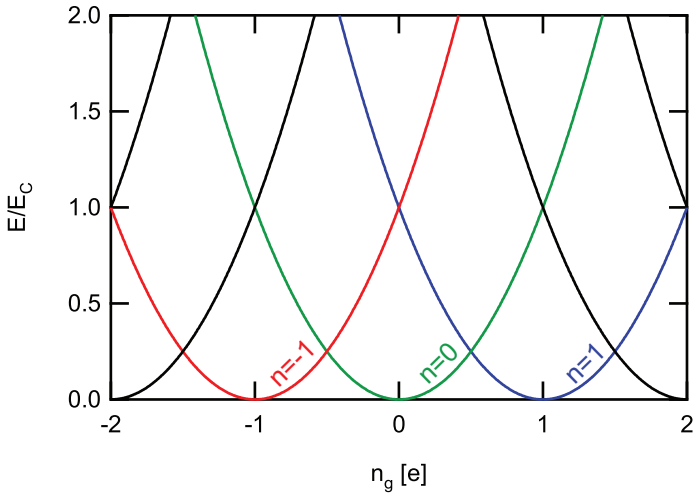

Figure 2.2: Energy levels of the single electron box. The Coulomb energies for several values of the charge state on the box, n, are plotted as a function of applied gate charge. The points at which these curves cross are the charge degeneracy points, at which the charge on the box will increment by one electron, to remain in the ground state.

parabolas as a function of gate charge that cross at the charge degeneracy points, $n_g = 1/2, 3/2, \ldots$. In the absence of thermal or quantum fluctuations, the charge on the box increases in a stepwise fashion by one electron at exactly these charge degeneracy points. This staircase is the stability diagram for the trap as it indicates the ground state of the circuit as a function of the control gate. At finite temperature, thermal fluctuations allow excursions out of the ground state. The average

charge on the island is then described by a Boltzmann weighted average of charge states

$$\langle n \rangle = \frac{\sum_{n=-\infty}^{\infty} n \ \exp(-E_n/k_B T)}{\sum_{n=-\infty}^{\infty} \exp(-E_n/k_B T)} \tag{2.2}$$

Away from the zero temperature limit, the average charge is no longer discretely quantized and the staircase becomes broadened. We can rewrite this formula in terms of a dimensionless parameter χ.

$$\chi = \frac{2k_B T}{E_C} \tag{2.3}$$

$$\langle n \rangle = \frac{\sum_{n=-\infty}^{\infty} n \ \exp(-2\chi(n-n_g)^2)}{\sum_{n=-\infty}^{\infty} \exp(-2\chi(n-n_g)^2)} \tag{2.4}$$

Plotting $1/\chi$ versus the temperature give us a way to fit the measurements to extract the charging energy of the box and observe any electron temperature saturation at low temperatures. Figure 2.3 shows a plot of the Coulomb staircase for several values of χ, which was first measured by Lafarge, et al. [LAFARGE1991] at Saclay in 1991. Note that even though the average charge n is not quantized

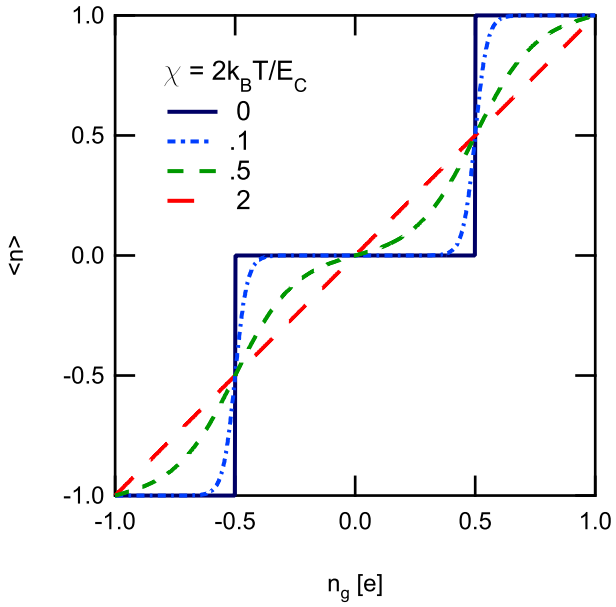

Figure 2.3: Coulomb staircase for several values of the dimensionless parameter χ. The average charge on the box island is plotted as a function of applied gate charge $n_g = C_g V_g/e$. Note that at $\chi = 2$, the temperatures is equal to the charging energy.

at finite temperatures, the instantaneous charge n remains quantized. For example, at $n_g = 1/2$, we would measure $\langle n \rangle = 1/2$, but the charge on the box is rapidly switching between 0 and 1, spending an equal amount of time in each state. The typical rates in this circuit are always in the range of 50 MHz - 1 GHz regardless of temperature, which is too fast to be able to time resolve the single tunneling events. In addition to the thermal fluctuations in this circuit, there are also quantum fluctuations, or cotunneling. I will discuss this in more detail for the single electron trap in Chapter 5, it should be noted that they also occur in the box and have been measured to high precision by Lehnert, et al [Lehnert2003]. I will discuss the details of the rate calculations in Chapter 4, and we will find that we need a more complex circuit to slow the electrons down to the range that is measurable with the RF-SET (discussed in detail in Chapter 3). In the next section, I will introduce the single electron trap which has rates that are tunable down into a measurable range.

2.2 Statics in the Single Electron Trap

The single electron trap circuit is the next level up in complexity from the single electron box. The trap, shown in Figure 2.4a, consists of an intermediate island with charge n_{Isl} and a trap island with charge n_{Trap}. This circuit has two gate voltages to bias these islands, each applying gate charges

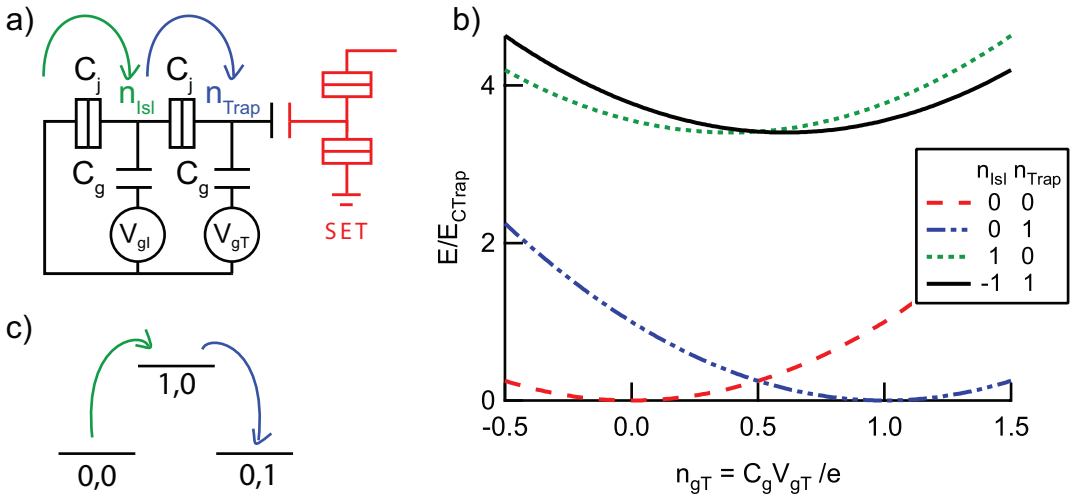

Figure 2.4: a) Circuit diagram of the single electron trap. b) Energy level diagram as a function of trap gate charge n_{gT} at island gate charge $n_{gI} = 0$ showing the four lowest charge states for the trap near the trap energy degeneracy point $n_{gT} = 1/2$ normalized by the trap charging energy. This is calculated for a circuit with trap charging energy 0.7 K and island charging energy 2.5 K. c) The charge configuration space picture of the trap shows how the electrons must go up hill both ways to reach the trap.

$n_{gi} = C_{gi}V_{gi}/e$. The energy level diagram for a trap with $E_{CIsl} = 2.5\ K$ and $E_{CTrap} = .7\ K$ at a gate charge $n_{gI} = 1/2$ is shown in Figure 2.4b as a function of n_{gT}. This diagram has a parabolic shape similar to that of the box but with one important difference. The presence of the intermediate island adds an additional energy level that the electrons must overcome. Electrons can be added onto the trap island in one of two ways. One possibility is that an electron can tunnel first onto the intermediate island and then onto the trap island:

$$(n_{Isl}, n_{Trap}) = (0,0) \rightarrow (1,0) \rightarrow (0,1) \tag{2.5}$$

The other possibility is that the order of the tunneling events can be reversed with an electron tunneling from the island to the trap, and another electron tunneling from the reservoir onto the island:

$$(n_{Isl}, n_{Trap}) = (0,0) \rightarrow (-1,1) \rightarrow (0,1) \tag{2.6}$$

At the trap charge degeneracy point, $n_{gT} = 1/2$, each of these paths corresponds to tunneling into an energetically forbidden level, shown in the charge configuration picture (Figure 2.4c). The same is true for the reverse rate to tunnel from the trap back to the reservoir, so the electrons must travel *up hill both ways* on and off of the trap island.

The time averaged behavior of the trap is similar to the single electron box, except that the stability diagram has a third dimension which is the extra gate. The stability diagram of charge as a function of each gate forms a hexagon pattern which is shown for the idealized zero temperature limit in Figure 2.5. The hexagon pattern of charge is closely related to the well-known hexagonal patterns in conductance previously observed in single-electron pumps [POTHIER1992] and turnstiles [URBINA1991] as well as those observed in double quantum dots [Wiel2003, Chan2003, Fujisawa2006, Sigrist2006]. The boundaries between the hexagons are the locations in the gate bias space where the charge on one of the two islands changes by one, and the hexagons can then be identified by the indexing (n_{isl}, n_{trap}) shown. As with all metallic single electron devices, the actual number of electrons on each island is very large, so the choice of zero is arbitrary. This pattern also provides a mapping of the gate settings to allow us to correctly bias the circuit.

Measuring the average charge on the trap island as a function of n_{gT} at $n_{gI} = 0$ gives the Coulomb staircase as was shown in Figure 2.3 for the box. The tunneling rates in the trap become significantly slower than those in the box at the degeneracy point due to the fact that there is an energetically forbidden state between the cells of the honeycomb. Because of the extra island, the

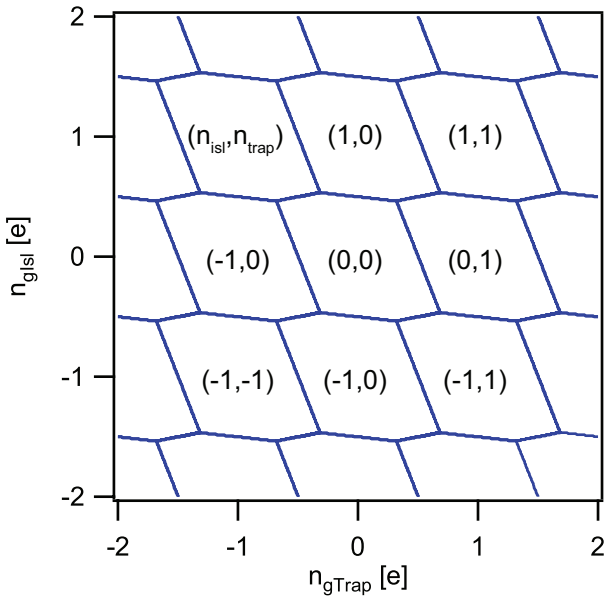

Figure 2.5: Idealized zero temperature stability diagram of the single electron trap. Plotted is the ground state of the single electron trap as a function of both gate voltages. The lines of the hexagons correspond to the locations in gate charge where the charge on one of the islands changes by one electron. This model is calculated for a trap circuit with trap charging energy of 0.7 K and island charging energy of 2.5 K.

characteristic rates for this circuit can be brought down into the range of 500 Hz-1 MHz which is slow enough to be detected with the RF-SET. The rates depend on energy differences between the charge states which are determined by the charging energies of the islands and the settings of the gate voltages. Our ability to tune the rates within this range will be determined both by our circuit design and by our ability to tune the gate voltages with some precision.

To go beyond the many experiments that measure statics in these systems, one needs to develop an understanding of the dynamics. The other important aspect of the experiments will be the charge detection, implemented using the RF-SET. Chapter 3 introduces the single electron transistor and the techniques used for rapid charge measurement. Also presented are figures of merit for judging the viability of detection of single tunneling events in various circuits based on sensitivity and maximum detectable tunneling rates.

Chapter 3

Charge Detection with the RF-SET

3.1 Introduction to the Single Electron Transistor

The single electron transistor (Figure 3.1) consists of two ultra-small tunnel junctions ($50 \times 50\ nm$) with resistances $R_{1,2} >> R_K$ in series with a small metallic island ($100\ nm \times 1\ \mu m$). This device was first proposed in 1986 by Averin and Likharev [AVERIN1986], and the first experimental realization was in 1987 at Bell Laboratories by Fultan and Dolan [FULTON1987]. We call this device a single

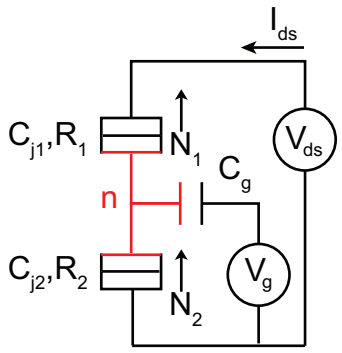

Figure 3.1: The circuit diagram of the SET. The SET consists of two small tunnel junctions in series with an island between them. Current, I_{ds}, flows through the transistor. The charge state of the island takes on discrete values, n, and electrons tunnel on and off of the island one by one. The number of electrons that have tunneled through the first and second junction are $N1$ and $N2$.

electron *transistor* because the current flow through the device is modulated by a gate voltage. We borrow the nomenclature from field-effect transistors (FETs) and say that it is voltage biased through the drain and grounded through the source and the electrostatic energy of the circuit is adjusted through a gate coupled nearby. At temperatures lower than the charging energy of the SET,

electrons flow one by one from source to drain. The SET functions much like the single electron box at $V_{ds} = 0$. The number of excess electrons on the SET island, n, changes when electrons tunnel through either junction. The total number of electrons that have tunneled through each of the junctions are N_1 and N_2. We can write this in terms of a charge advance number k, which will allow us to write down the current through the transistor:

$$k = \frac{N_1 + N_2}{2} \tag{3.1}$$

$$I_{ds} = e\left\langle \frac{dk}{dt} \right\rangle \tag{3.2}$$

Just as in the trap and the box the number of electrons on the island switches between two charge states:

$$n \rightarrow n+1 \rightarrow n \rightarrow n+1 \rightarrow n \rightarrow n+1 \ldots \tag{3.3}$$

In the SET the frequency of tunneling events is related to the total drain-source current, f=I/e $\sim$ GHz. This is too high to time resolve, but we will exploit other properties of the SET, using it as a fast sensitive electrometer in order to detect single tunneling events on the trap.

Electrons can only tunnel onto the SET island when it is energetically allowed. The total electrostatic energy of the SET depends on n, the drain-source voltage V_{ds}, and the applied gate charge $n_g = C_g V_g$ and is given by

$$E = E_C(n - C_{j1}V_{ds}/e - n_g)^2 \tag{3.4}$$

plus terms that do not depend on the number of electrons on the island which have been dropped (energy differences between states determine whether or not tunneling will occur, so the other terms will cancel out). With no applied gate voltage, at $V_{ds} = 0$, tunneling is energetically forbidden and we have what is called Coulomb blockade. This is shown in the center region of the blue curve in Figure 3.2. This blockade can be lifted with the correct potential applied to any nearby electrode or gate allowing current to flow through the SET, turning on the transistor. The potential required is $e/2C_g$ or half of an electron of gate charge $q_g = C_g V_g$. The maximum and minimum values of the blockade are shown in Figure 3.2, which determines the amount of modulation in a current measurement taken at a particular bias point. Just as in the box, the gate charge is a continuous variable, and the behavior of the SET is periodic in gate charge, with a periodicity of one electron. Figure 3.3 shows the current through the SET as a function of V_g.

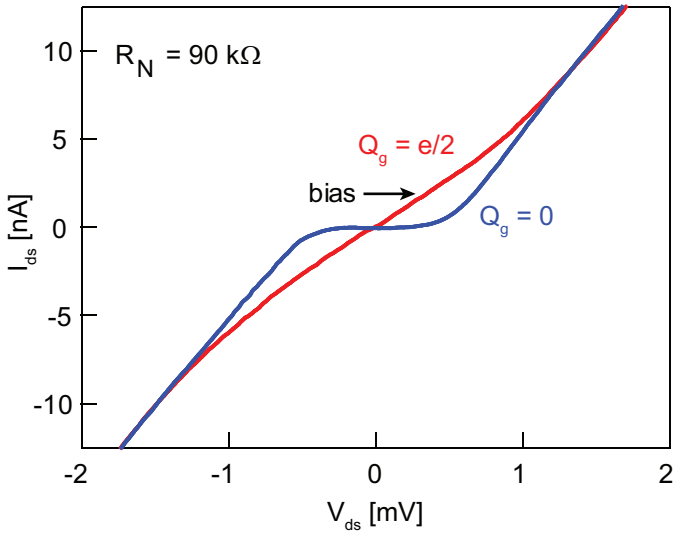

Figure 3.2: Drain-source current, I_{ds} through the SET measured as a function of drain-source voltage, V_{ds}. At zero applied gate charge, $Q_g = 0$, around $V_{ds} = 0$, tunneling is energetically forbidden, so no current can flow, and we have what is called Coulomb blockade (blue curve). This blockade can be lifted with the correct applied gate charge, $Q_g = e/2$, shown in red, and the I-V curve becomes nearly linear. A particular bias point is indicated by the arrow where the current through the SET is dependent on any changes in the applied gate charge, and the SET can be operated as an electrometer. This particular curve is for an SET with a normal state resistance $R_N = 90k\Omega$.

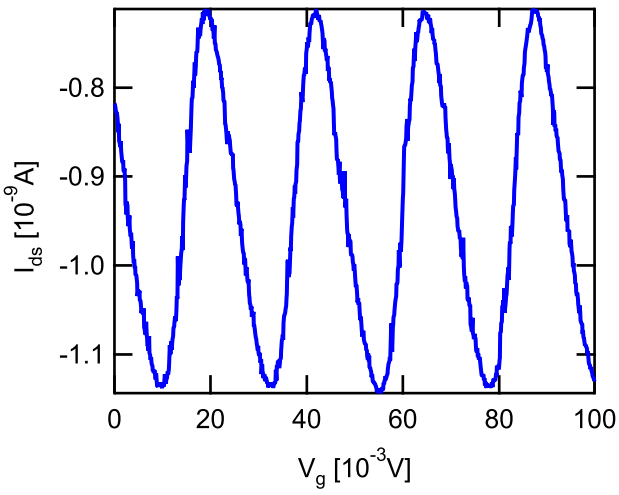

Figure 3.3: Drain-source current through the SET measured as a function of gate voltage. The gate capacitance can be calibrated using the fact that the SET signal has a period of 1 electron. The SET is used as a sensitive electrometer when it is biased anywhere there is a measurable slope in the current as a function of gate voltage.

The high sensitivity of the SET current to gate charge, or any charge coupled nearby is what allows the SET to act as a sensitive electrometer. Figure 3.4 shows an example of this with the SET capacitively coupled to the island of a single electron box. A typical SET measurement detects a

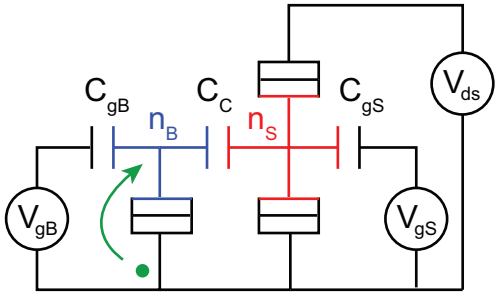

Figure 3.4: The SET capacitively coupled, via C_C to a single electron box. The blue lines denote box island with n_B electrons and the red lines denote the island of the SET with n_S electrons. The green dot indicates the signal being measured by the SET, which is a single electron tunneling onto the box island.

change in potential corresponding to a gate charge of approximately $10^{-4}\ e/\sqrt{Hz}$. The high output impedance, which is at least on the order of $R_K = h/e^2 \sim 26\ k\Omega$, however, limits measurements to the kHz range. The next section will discuss high frequency measurement techniques that increase both the bandwidth and the sensitivity of the SET.

3.2 High frequency measurements

The long RC time due to the high impedance SET and capacitance of the cables limit measurements to the kHz range of measurement frequencies. The low frequency operation of these devices also limits their sensitivity, since measurements are made in the rage of high 1/f noise due to the motion of charge impurities in the substrate and tunnel barriers. The radio frequency SET (RF-SET) measurement technique works around these both of these problems by embedding the SET in a resonant LC circuit (shown in Figure 3.5) [Schoelkopf1998]. With this setup, we measure the change in damping of the resonant circuit due to changes in drain-source current through the transistor. Measuring the reflected power is an analogous to measuring the conductance through the device. This device has demonstrated measurement bandwidths of greater than 100 MHz. The sensitivity is also greatly improved, giving charge noise measurements as low as $5 \times 10^{-6}\ e/\sqrt{Hz}$ [Devoret2000]. Faster bandwidth equates to shorter integration times, which also improves the sensitivity.

The response of the SET circuit as a function of V_{ds} and V_g is shown in Figure 3.6. This is

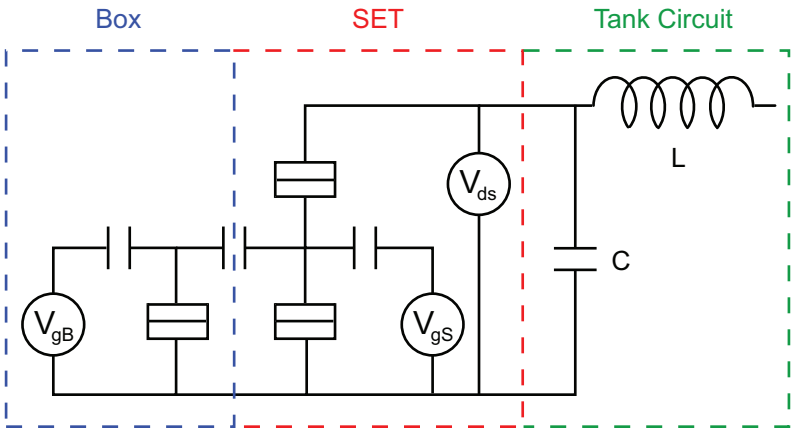

Figure 3.5: Schematic of the RF-SET with microwave circuitry. The single electron box is capacitively coupled to the SET just as in the previous figure. The high frequency measurements are performed with the SET embedded in an LC resonant circuit.

known as the Coulomb diamond. The black areas of the figure indicate low conductance and the SET is blockaded in a single charge states within these diamonds. The white numbers indicate the charge on the SET in these regions. The slant in the diamond pattern, indicated by the ratio of slopes of the green dashed lines in the figure, indicates the degree of symmetry of the capacitances of the two junctions. The SET can be biased anywhere on this diagram where there is a color change in the horizontal direction. Those are the locations where the SET is sensitive to small changes in gate voltage and can thus be used as an electrometer. A particular choice for the operating point is indicated by a white dot in Figure 3.6.

The important quantity in this measurement is the strength of the coupling capacitor which is the amount of polarization charge induced on the SET island due to a change of one electron on the capacitively coupled circuit such as the single electron box. The signal size is $q_{sig} = \kappa e$, where $\kappa = C_C/C_{S_\Sigma}$ (see Figure 3.4) is the dimensionless coupling ratio of the coupling capacitance of the two islands to the sum capacitance of the box island. A typical coupling strength of 10% allows for resolution of single tunneling events in the time domain with a signal to noise ratio of 1 with a maximum bandwidth $B_{max} = \kappa^2/S_q \sim 2\ MHz$, if we assume a charge sensitivity of $7 \times 10^{-5} e/\sqrt{Hz}$[1]. This number B_{max}=2MHz will serve as a high frequency cut-off for evaluating the feasibility of measurements of time resolved tunneling events in various circuits. We will look for a circuit that has tunneling in a range of frequencies that are far below this maximum bandwidth.

[1]Note that the units here are not Coulombs$^2/Hz$, but e^2/Hz, which gives the correct dimensionality for the bandwidth.

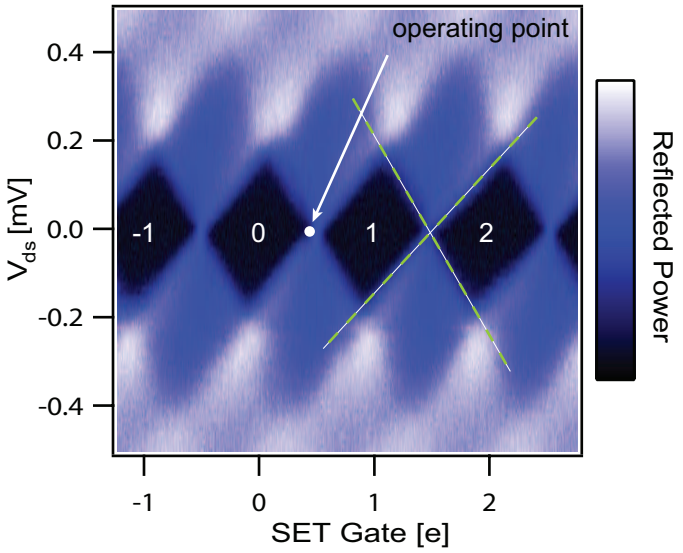

Figure 3.6: Coulomb diamond of the SET. Reflected power is plotted as a function of drain source voltage V_{ds} and SET gate charge, showing areas of conductance (blue-white) and areas of Coulomb blockade (black). Within these black diamonds, the SET is blockaded in a single charge state, and the white numbers indicate the charge on the SET island in these regions. The ratio of the slopes of the two green lines can be indicates the amount of capacitance asymmetry between the two tunnel junctions. The SET is sensitive to changes in gate voltage anywhere in the diagram where there is a color change in the horizonal direction. One particular operating point of the SET as an electrometer is indicated by the white dot.

More specific details of the RF measurement setup will be given in Chapter 7. Now that I have introduced the RF-SET, I will use the terms SET and RF-SET interchangeably and future references to the SET should not be confused with the dc-SET.

3.3 Measuring the Charge on the Single Electron Box

This section outlines the process of using the RF-SET as an electrometer to measure the average charge on the single electron box. It will be important to understand the mechanics of the measurement process to be able to evaluate the feasibility of measuring proposed circuits. I have already stated, and will show in Chapter 4, that the tunneling rates in the box are too fast to be time resolved by the SET. Nonetheless it is important to see how the number of islands in the problem affects the complexity of the measurements.

The circuit diagram shown in Figure 3.1 does not tell the whole story of the box-SET coupling. Realizing this circuit diagram in an actual thin-film circuit results in extra capacitances not typically drawn into the diagram. Figure 3.7 shows the more complete circuit diagram with the added parasitic capacitances and Figure 3.8 is an SEM micrograph of a real device. The procedure for measuring

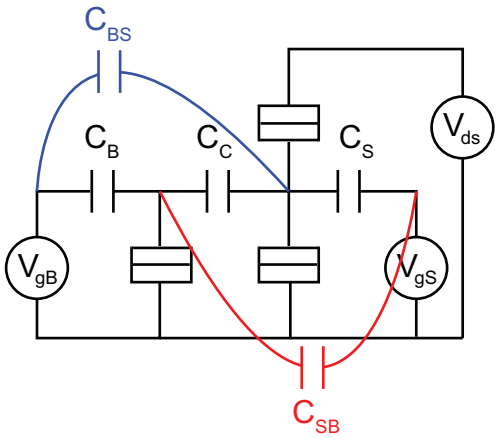

Figure 3.7: The full circuit diagram of a single electron box coupled to a single electron transistor. The extra capacitances in this diagram, C_{SB} and C_{BS}, are parasitic, or unwanted, cross capacitances of the gates to the opposite islands and have to be cancelled out in the operation of the experiment.

the charge on the box is to sweep the applied box gate charge and measure the response of the SET. We are unable to fabricate isolated gates that bias each island independently (see Chapter 6 for more details), so when the box gate is swept, it changes the operating point of the SET. A measurement that keeps the operating point of the SET constant involves finding the capacitance

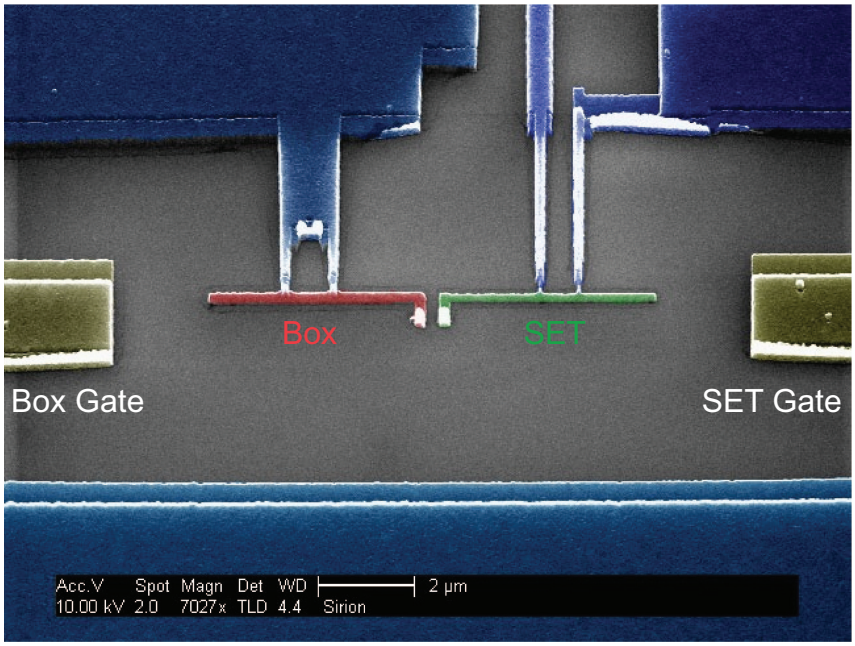

Figure 3.8: SEM micrograph showing a single electron box coupled to a single electron transistor fabricated at Yale by Johannes Majer. In this device, the capacitive coupling of the box gate to the box is nearly equal to that of the box gate to the SET. Independent biasing of the gates requires the gate biasing procedure described in the text.

matrix of the circuit and applying a gate voltage to the SET island to cancel the effects of the direct capacitance from the box gate to the SET island. The total charge applied to the two islands by the gate voltages is given by:

$$\begin{pmatrix} q_{gS} \\ q_{gB} \end{pmatrix} = \begin{pmatrix} C_S & C_{BS} \\ C_{SB} & C_B \end{pmatrix} \begin{pmatrix} V_{gS} \\ V_{gB} \end{pmatrix} \tag{3.5}$$

The gate charges are more typically expressed in terms of number of electrons $n_{gSET} = q_{gSET}/e$, or

$$\begin{pmatrix} n_{gS} \\ n_{gB} \end{pmatrix} = \frac{1}{e} \begin{pmatrix} C_S & C_{BS} \\ C_{SB} & C_B \end{pmatrix} \begin{pmatrix} V_{gS} \\ V_{gB} \end{pmatrix} \tag{3.6}$$

Starting out, all of the elements of the capacitance matrix are unknown. Simulations provide us with a starting point (see Chapter 6), but we require a much more precise characterization of the circuit in order to proceed. This formulation will be done assuming C_C is small enough that the signal q_{sig} from electron tunneling is a small perturbation on the SET response.

The first step is to find the capacitance of the SET gate to the SET island (C_S). To do this, we apply a voltage ramp corresponding to several electrons in gate charge to the SET gate and measure the reflected power as a function of time. The applied voltage ramp and the measured reflected

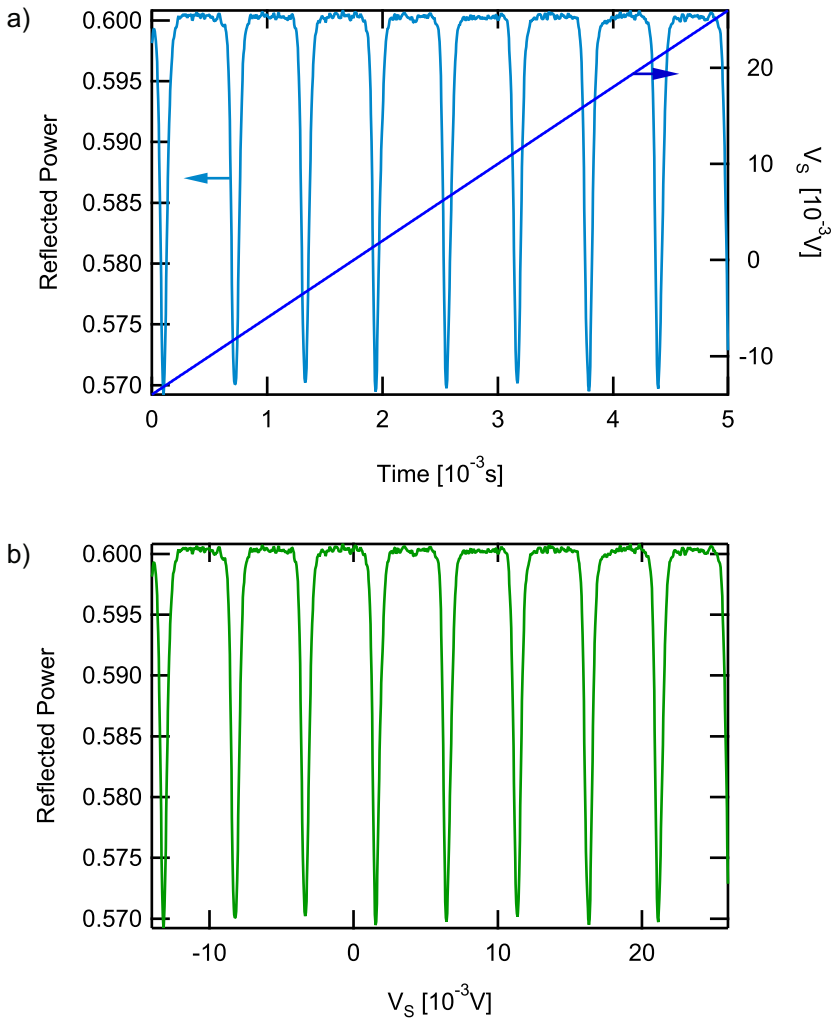

Figure 3.9: a) The applied gate voltage V_S is plotted as a function of time on the right axis while the measured reflected power signal is plotted on the left axis. b) Plotting these two quantities against each other gives the SET transfer function. The periodicity of the signal is one electron, and we find the SET gate capacitance $C_S = 32\ aF$.

power signal are shown in Figure 3.9a. We can re-plot this as SET response (reflected power) as a function of applied gate charge (Figure 3.9b). The SET response as a function of gate is called the SET transfer function. The periodicity is one electron, from which we can calibrate the SET gate capacitance. We repeat this measurement to find the capacitance of the box gate to the SET island, applying the voltage sweep to the box gate and measuring the response of the SET. We then have two elements of the capacitance matrix, C_S and C_{BS}.

To find the capacitances of each gate to the box island we apply a voltage sweep of magnitude $V_{gBox} = V_B$ and cancel this gate on the SET with a voltage sweep of $-\frac{C_{BS}}{C_S}V_B$. Plugging these into equation 3.6, we see that the SET charge remains constant allowing us to stay at the sensitive operating point:

$$\begin{pmatrix} n_{gS} \\ n_{gB} \end{pmatrix} = \frac{1}{e}\begin{pmatrix} C_S & C_{BS} \\ C_{SB} & C_B \end{pmatrix}\begin{pmatrix} -\frac{C_{BS}}{C_S}V_B \\ V_B \end{pmatrix} = \frac{1}{e}\begin{pmatrix} 0 \\ V_B\left(C_B - \frac{C_{SB}C_{BS}}{C_S}\right) \end{pmatrix} \tag{3.7}$$

The signal measured on the SET will be due to the changing average charge on the box island. The resulting graph is a sawtooth, shown in Figure 3.10. We get this function because the average

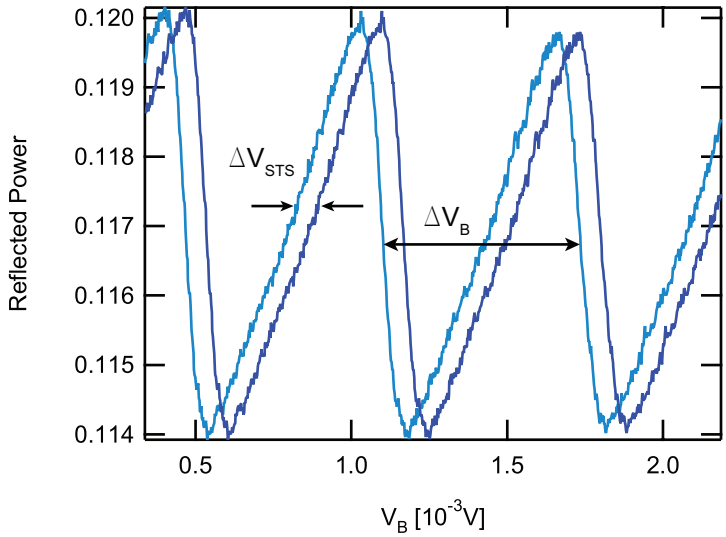

Figure 3.10: The raw measurement of the sawtooth for the single electron box. The single electron box has a periodicity of one electron, $\Delta V_B = 1e$. The second sawtooth comes from shifting the SET gate by a small amount Δq and measuring the resulting sawtooth shift (STS) ΔV_{STS}.

behavior of the box is that the capacitor is charged by the gate voltage increasing the potential on the box island until an electron tunnels at the charge degeneracy point and the box is reset. Setting

the period of the sawtooth, ΔV_B, equal to one electron, we find

$$\Delta V_B = \frac{e}{C_B - C_{SB}C_{BS}/C_S} \tag{3.8}$$

This is not enough yet to get both capacitances out. We have two unknowns so we need one more equation. Adding a small dc shift, Δq, to the SET voltage shifts the sawtooth by a small amount in apparent box gate voltage, $V_B = \Delta V_{STS}$.

$$\begin{pmatrix} n_{gS} \\ n_{gB} \end{pmatrix} = \frac{1}{e}\begin{pmatrix} C_S & C_{BS} \\ C_{SB} & C_B \end{pmatrix}\begin{pmatrix} -\frac{C_{BS}}{C_S}V_B + \frac{\Delta q}{C_S} \\ V_B \end{pmatrix} \tag{3.9}$$

$$= \frac{1}{e}\begin{pmatrix} \Delta q \\ \frac{C_{SB}\Delta q}{C_S} + V_B\left(C_B - \frac{C_{SB}C_{BS}}{C_S}\right) \end{pmatrix} \tag{3.10}$$

$$\Delta V_{STS} = -\frac{C_{SB}\Delta q}{C_S C_B - C_{SB}C_{BS}} \tag{3.11}$$

This gives us two equations with the last two capacitances as unknowns. Solving these for the last two capacitances we have

$$C_B = e\left(\frac{\Delta q - C_{BS}\ \Delta V_{STS}}{\Delta q\ \Delta V_B}\right) \tag{3.12}$$

$$C_{SB} = -\frac{e\ C_S \Delta V_{STS}}{\Delta q\ \Delta V_B} \tag{3.13}$$

Now that we have each element in the capacitance matrix, we can sweep the box gate some number of electrons while keeping the SET at a fixed bias. The end goal is a measurement of average charge on the box as a function of box gate, but what is directly measured is the reflected power signal from the SET as a function of box gate. The SET transfer function provides a mapping between reflected power and charge on the SET, and we make a lookup table to map between these two quantities (Figure 3.11). The resulting sawtooth is shown in Figure 3.12. From this measurement we can infer the charge on the box and construct the Coulomb staircase,

$$Q_B = \frac{n_{gB}e\kappa - Q_{SET}}{\kappa} \tag{3.14}$$

The inferred staircase is shown in Figure 3.13, measured at several temperature.s

The number of elements in the capacitance matrix, all unknown, is equal to the square of the number of islands in the circuit. The SET-box circuit has two islands and 4 unknown elements. We measure the charge on the box directly with the SET and are able to determine all four elements. The single electron trap has one island directly coupled to the SET, but the circuit has three islands and three gates. The capacitance matrix contains nine elements, but since we do not have direct

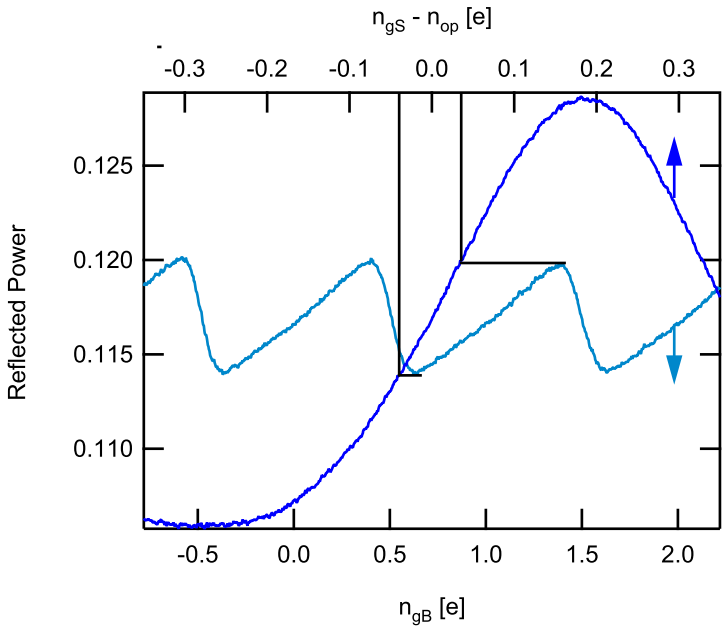

Figure 3.11: The raw measurement of the sawtooth for the single electron box and the mapping from reflected power to charge on the SET island.

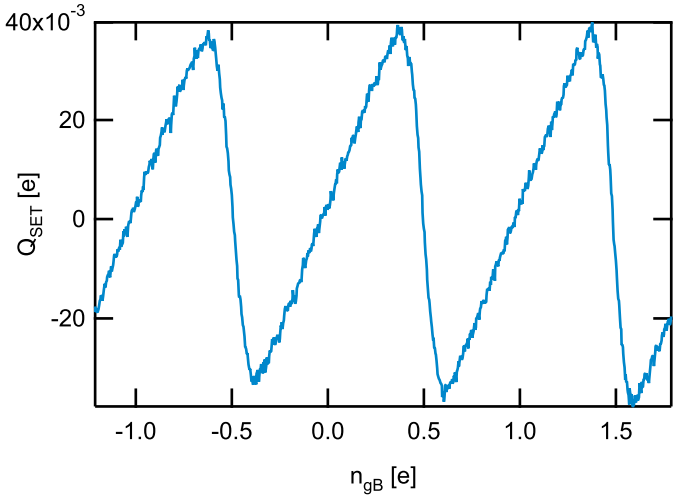

Figure 3.12: The sawtooth of the single electron box. Here we plot the charge on the SET as a function of applied gate charge on the box.

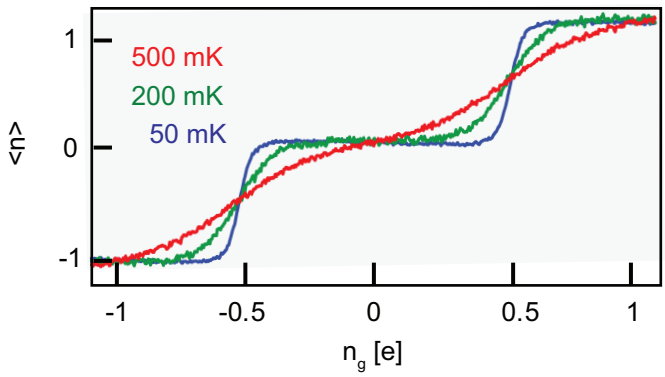

Figure 3.13: Measurements of a staircase of a single electron box with charging energy 1.6 K performed by Konrad Lehnert at several temperatures.

access to the intermediate island, the determination of the additional elements becomes much more complicated. If it is important to determine all of the elements of the capacitance matrix in order to effectively perform an experiment, then it would be wise to limit the number of islands and gates that must be characterized. Chapter 6 of this thesis goes into more detail on the design elements of the trap experiment that aim to simplify the measurement process. But first, Chapters 4 and 5 discuss the rate calculations that will go into the circuit designs.

Chapter 4

The Sequential Tunnelling Model

4.1 Introduction

This chapter presents the framework for calculating the rates using the sequential tunneling model. After an overview of the model, calculations will be shown for the single electron box and the single electron trap. We will see at the end of this chapter that there is more to learn about the tunneling rates, and this will take us to the next chapter which will discuss the quantum fluctuations. This first order calculation is more straightforward, and will provide a first cut with which we can filter out prospective circuits. We will compare results found in this chapter to the figure of merit for the SET (SNR=1 $<$ 2MHz) explained in the preceding chapter.

4.2 Orthodox Theory

The total tunneling rate across a junction will be calculated in the framework of the "global rule", or "orthodox theory" which was established by [NAZAROV1989, Devoret1990, Girvin1990, GRABERT1991]. This framework has been widely used, for example, to calculate measurable quantities such as the current-voltage characteristics of tunnel junctions at finite temperatures [Devoret1990, INGOLD1991] and predict the backaction of the single electron transistor onto a single electron box [Turek2005]. The global rule states that the probability for tunneling is a function of the entire state of the environment in which the circuit is embedded. In the case of the experiments in this thesis, the impedance of the environment is small compared with the resistance quantum, R_K, and we will have a special case of the overall framework of rate calculations explored in the references above. In this case, the first order calculations simplify to the rate calculated using conventional techniques neglecting the coupling of the circuit to the environment (see e.g. Tinkham

[Tinkham1996]). In this approach, we assume that tunneling occurs only through sequential tunneling events, and that multiple tunneling events, or cotunneling (explored in more detail in the next chapter) are negligible. We also assume that the tunneling is an uncorrelated stochastic process. The sequential tunneling rate depends only on the energy difference between the initial and final states of the circuit before and after the tunneling event has occurred.

The rate for an electron to tunnel across a junction is calculated using Fermi's golden rule. From Sakurai [Sakurai1994], the rate for a transition between two single particle states i and f is given by

$$\Gamma_{i\to f} = \frac{2\pi}{\hbar}\sum_f |T_{if}|^2\delta(\epsilon_f - \epsilon_i) \tag{4.1}$$

where $|T_{if}|$ is the matrix element for this transition and ϵ_i and ϵ_f are the energies of the electrons in the initial and final states. This expression is integrated over the total density of states $\int E_n\rho(E_n)$ available to a tunneling electron. In our case, for single tunneling events across a high impedance (with respect to R_K) tunnel junction in a low impedance environment, this matrix element is equal to an average value describing the barrier. To obtain the total tunneling rate across the junction, we assume that the density of states on each side of the junction is constant as a function of energy, and integrate over all possible energies. The probability that there is a filled state on the left side of the junction is just the Fermi function,

$$f(\epsilon) = \frac{1}{1 + exp(-\beta\epsilon)} \tag{4.2}$$

where $\beta = 1/k_BT$, and the probability that there is an unfilled state on the right hand side is $[1 - f(\epsilon)]$. The total tunneling rate across the junction from left to right is then

$$\Gamma_{L\to R} = \frac{g}{h}\int_{-\infty}^{\infty} f(\epsilon)[1 - f(\epsilon')]d\epsilon d\epsilon' \tag{4.3}$$

This expression can be integrated analytically yielding a Bosonic type expression, essentially the rate to create an electron hole pair

$$= \frac{g}{h}\frac{\Delta E}{1 - exp(-\beta\Delta E)} \tag{4.4}$$

where ΔE is the total energy difference between the initial and final states of the circuit and $g = h/e^2R_j$ is the dimensionless conductance of the junction. A dimensionless conductance of 1 corresponds to a junction resistance of 25.8 $k\Omega$. At zero temperature, tunneling is forbidden for negative $\Delta E_{n-n'}$ but at finite temperatures, tunneling becomes energetically allowed at even

negative energy differences due to thermal fluctuations. Tunneling rates as a function of $\Delta E_{n-n'}$ are shown in Figure 4.1, assuming $g = 1$.

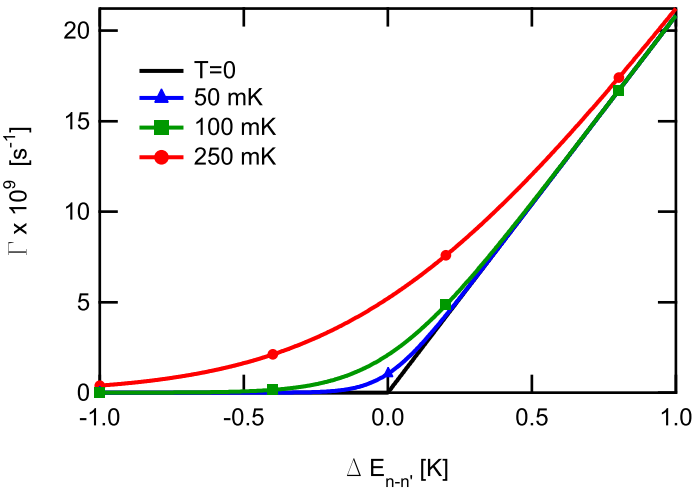

Figure 4.1: Orthodox theory tunneling rates as a function of the energy difference between charge states n and n' for $g = 1$. Increased temperature allows energetically forbidden transitions at negative energy differences. At $\Delta E_{n-n'} = 0$, the rates are linear in temperature and go as gk_BT/h.

4.3 Tunnelling Rates in the Single Electron Box

The total electrostatic energy in the single electron box is given by

$$E(n, n_g) = E_C(n - n_g)^2 \tag{4.5}$$

and the rate to tunnel between two states n and n' is written

$$\Gamma = \frac{g}{2\pi} \frac{\Delta E_{n-n'}/\hbar}{1 - exp(-\Delta E_{n-n'}/k_BT)} \tag{4.6}$$

For temperatures that are small compared with E_C, in the range of $n_g = [0, 1]$, we only need to consider the two lowest energy states, with charge 0 and 1, as shown in Figure 4.2. At the charge degeneracy point, $n_g = 1/2$, we would measure the average charge on the box to be $\langle n \rangle = 1/2$ (see Figure 2.3) with n, the instantaneous charge on the box island, fluctuating rapidly between 0 and 1 with a 50% duty cycle. If we were able to time resolve this perfectly, we would see telegraph noise that looked like Figure 4.3a. Moving away from this point would change the duty cycle as shown in Figure 4.3b. This would slow one of the rates, but would significantly increase the other toward the limit that the telegraph noise would resemble a series of delta functions. Tunneling

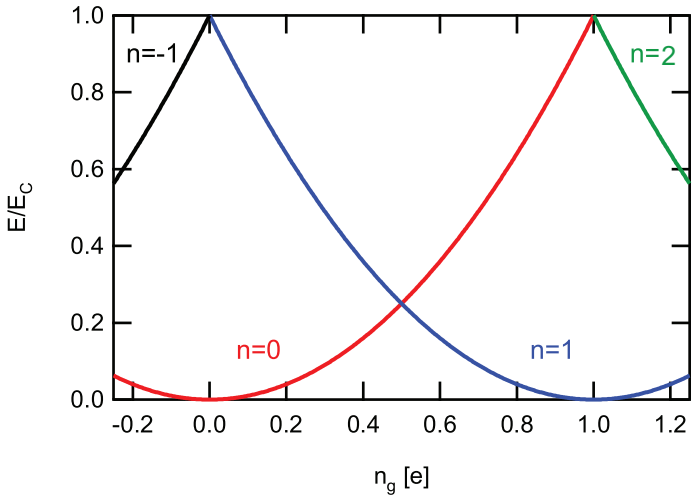

Figure 4.2: Energy level diagram for the single electron box. The Coulomb energy is plotted as a function of the applied gate charge $n_g = C_g V_g/e$ for four charge states of the single electron box. The energy levels are quadratic in gate charge and cross at the charge degeneracy points.

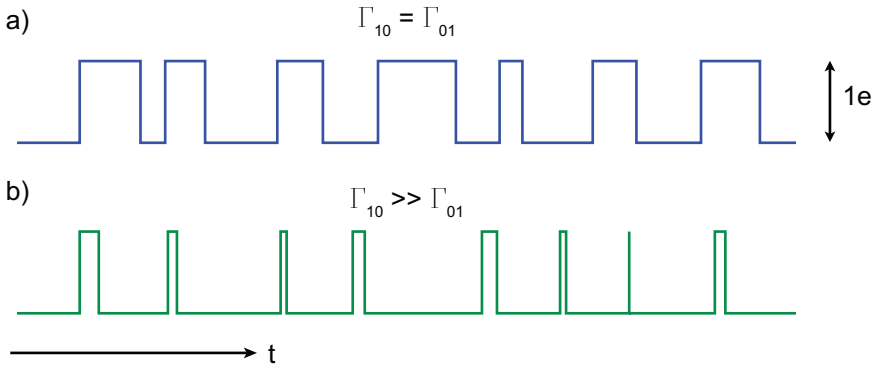

Figure 4.3: Charge fluctuations between two charge states, known as telegraph noise. a) Telegraph noise at charge degeneracy with 50% duty cycle is the easiest to detect. b) Far from charge degeneracy the rate to go from 0 to 1 is slower, but the reverse rate is much faster. The chance to miss events in the detection scheme becomes higher.

rates as a function of temperature are shown for a gate bias of 0.7e as a function of temperature in Figure 4.4. The tunneling rate from the ground state to the excited state is suppressed at low temperature, and can be made quite small, but this comes at the price of the return rate staying at an almost constant high rate (500 MHz at 50 mK) for a box with charging energy $E_C = 0.7\ K$ and a dimensionless conductance of 0.1. The best case scenario for any detection scheme would be

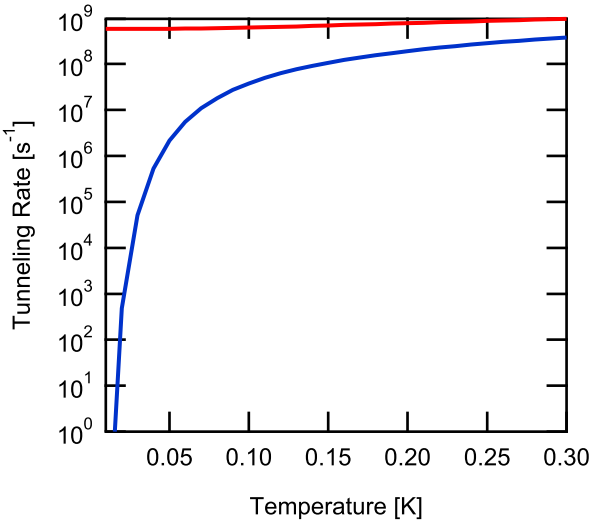

Figure 4.4: Tunneling rates as a function of temperature in the single electron box plotted at gate charge $n_g = 0.7e$. The rate to tunnel from the ground state to the excited state (in this case n=1 to n=0) is suppressed at low temperatures. This slow tunneling rate comes at the price of a high reverse tunneling rate from the excited state back to the ground state that is nearly independent of temperature. At 50 mK, this rate is still at 500 MHz. The charge on the box is almost always in the ground state, with rare, short excursions into the excited state.

to have equal tunneling rates on and off the island, with the electrons spending a maximal amount of time in either state. We will see that in all of the circuits, both rates are lowest at the charge degeneracy point.

To calculate the rates, we find the energy difference between the two applicable states

$$E(1) - E(0) = E_C(1 - 2n_g) \tag{4.7}$$

$$E(0) - E(1) = -E_C(1 - 2n_g). \tag{4.8}$$

The tunneling rates between the 0 and 1 states for a box with $E_C = 0.7\ K$ are shown as a function of gate charge in Figure 4.5a[1]. Figure 4.5b shows the temperature dependence of the tunneling rates

[1]The charging energy of the box shown in this example is chosen for ease of comparison with the single electron trap in the next section.

at the charge degeneracy point. The rates are far above the 2 MHz cutoff at all temperatures which

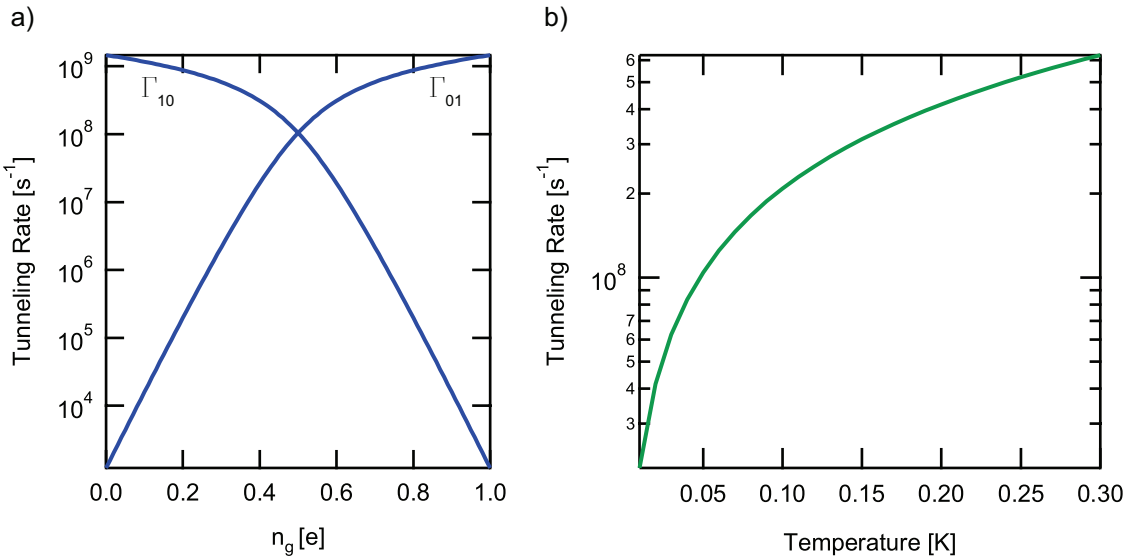

Figure 4.5: a) Orthodox theory tunneling rates for a single electron box with $E_C = 0.7\ K$ and $g = 0.10$ at $50\ mK$. b) The thermal rates in the box are plotted at the charge degeneracy point where the forward and reverse rates are equal. At charge degeneracy, the rates are linear in temperature and equal to gk_BT/h. Tunneling events are too rapid to be detected by the single electron transistor at any temperature.

we can see looking at the limiting behavior of the rate equation: as $T \to 0$, $\Gamma \to g\frac{\Delta E_{n-n'}}{h}$ and as $\Delta E_{n-n'} \to 0$, $\Gamma \to g\frac{k_BT}{h}$. The rates are linearly dependent on the dimensionless conductance, which in a metallic system is typically in the range $0.05 - 1$. Outside of this range, junction fabrication is difficult to control. It is also a fixed number in experiments with tunnel junctions, in contrast with a quantum dot with a tunable tunnel coupling.

4.4 Tunneling Rates in the single Electron Trap

The energy equation for the trap is slightly more complicated now that there are more islands involved. Due to the addition of the extra island, there are cross terms that have to be considered. Each piece of metal in the problem is considered to be a node. A simplified version of this picture along with the circuit diagram for the trap ignoring cross capacitances are shown in Figure 4.6. The cross capacitances will be be cancelled in the experiment, as outlined for the box in Chapter 4.

Following the formulation in [Lafarge1993], we write down the full capacitance matrix, $\mathbb{C}$, for the

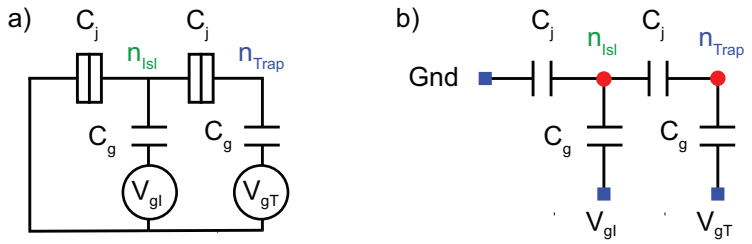

Figure 4.6: Schematic for the single electron trap. a) Circuit diagram for the single electron trap. b) Diagram showing the nodes used for the energy calculation. The red circles indicate the islands and the blue boxes indicate voltage sources. Cross capacitances between nodes that are not shown are assumed to be zero, which can be achieved through cancelling procedures similar to the one outlined in Chapter 3.

single electron trap. The matrix elements are

$$\mathbb{C}_{ii} = \sum_{i \neq j} C_{ij} \tag{4.9}$$

$$\mathbb{C}_{ij} = -C_{ij} \tag{4.10}$$

where C_{ij} is the direct capacitance between nodes i and j, where i, j are either islands or voltage sources. In general, the capacitance matrix $\mathbb{C}$ links the potential of the nodes v to the charge of the nodes q by

$$q = \mathbb{C}v \tag{4.11}$$

where q and v are vectors containing the charges and voltages, respectively, of the nodes of the circuit. The gate charges applied to the islands can be written as

$$\widetilde{q}_\alpha = \sum_s \mathbb{C}_{\alpha s} v_s \tag{4.12}$$

where s is the set of voltage sources and α are the islands.

I will drop terms in the energy equation that do not depend on the charges on the islands because the rates depend only on energy differences between charge states[2]. We take the subset of the capacitance matrix, $\widetilde{C}$

$$\widetilde{C}_{\alpha\beta} = \mathcal{C}_{\alpha,\beta} \tag{4.13}$$

for the set of α, β which are islands. The energy (including only the relevant terms) as a function of the charge on each island is

$$E = \frac{1}{2} \sum_{\alpha,\beta} \widetilde{C}^{-1}_{\alpha\beta} (n_\alpha - \widetilde{q}_\alpha)(n_\beta - \widetilde{q}_\beta) \tag{4.14}$$

[2]The more complete calculation that was done for the experiments in this thesis also includes the SET, which will be neglected here for simplicity. A full expression of the energy including the SET is given at the end of Chapter 5 in the discussion of the backaction of the SET

For the trap, this is

$$E = \frac{e^2}{2}\left(\widetilde{C}^{-1}_{1,1}(n_{Isl} - n_{gT})^2 + \widetilde{C}^{-1}_{2,2}(n_{Trap} - n_{gI})^2 + 2\widetilde{C}^{-1}_{1,2}(n_{Isl} - n_{gT})(n_{Trap} - n_{gI})\right). \quad (4.15)$$

Analyzing this equation, we can see that the charging energy of the island is

$$E_{CIsl} = \frac{e^2}{2}\widetilde{C}^{-1}_{2,2}. \quad (4.16)$$

and for the trap

$$E_{CTrap} = \frac{e^2}{2}\widetilde{C}^{-1}_{1,1} \quad (4.17)$$

We can rewrite the total electrostatic energy as

$$\begin{aligned} E &= E_{CTrap}(n_{Trap} - n_{gTrap})^2 + E_{CIsl}(n_{Isl} - n_{gIsl})^2 \quad (4.18)\\ &+ 2E_{Coup}(n_{Trap} - n_{gTrap})(n_{Isl} - n_{gIsl}) \end{aligned}$$

where E_{Coup} is the coupling energy between the two islands. This is similar to the single electron box with the addition of the extra cross term, which comes in from the fact that the excess charge one island acts as gate to the other island.

For temperatures that are low compared with the charging energies of both islands, $kT < E_{CTrap}, E_{CIsl}$, we can calculate the rates considering the four lowest energy levels, shown in Figure 4.7, which are $(n_{Isl}, n_{Trap}) = (0,0), (1,0), (-1,1)$, and $(0,1)$.

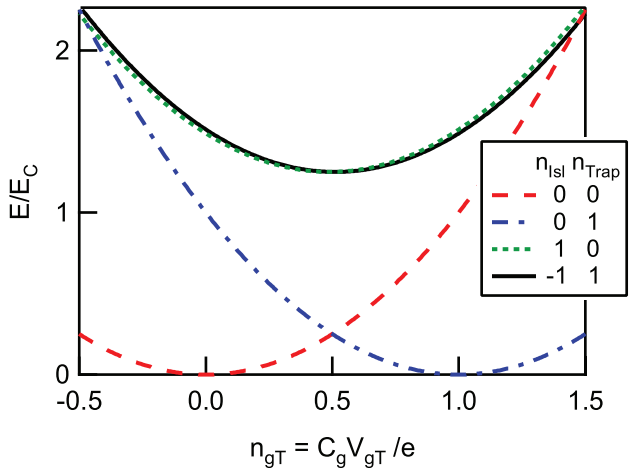

Figure 4.7: Coulomb energy level diagram showing the four lowest energy levels for the single electron trap, normalized to the charging energy of the trap, E_{CTrap}. This energy level diagram is achieved for a circuit with $E_{CIsl} = 2E_{CTrap} = 2K$ and shown for an island gate bias at $n_{gIsl} = 0$. The intermediate states (1,0) and (-1,1) have a high energy cost.

At $n_{gIsl} = 0$, and $n_{gTrap} = 1/2$, in order to change the charge state in the circuit from $(0, 0)$ to $(0, 1)$, we must first go either through state $(1, 0)$. An alternative is to tunnel through the second junction first, taking the path $(n_{Isl}, n_{Trap}) = (0, 0) \rightarrow (-1, 1) \rightarrow (0, 1)$. In order to transfer an electron from the reservoir to the trap island, we must first overcome a higher energy intermediate state. The rate for this process, which is energetically forbidden at zero temperature, is quite small. The total time for an electron to tunnel is the sum of the time to tunnel onto the island (long) plus the time to tunnel onto the trap (short). The second rate is very fast because the energy difference is positive and large. The total rate will be low since it is limited by the long time for the first tunneling event. The tunneling rate for the process proceeding through the first path is given by Γ_A

$$\Gamma_A = \frac{\Gamma_{(0,0)\rightarrow(1,0)}\Gamma_{(1,0)\rightarrow(0,1)}}{\Gamma_{(0,0)\rightarrow(1,0)} + \Gamma_{(1,0)\rightarrow(0,1)}} \tag{4.19}$$

The rate for the alternate path is given by Γ_B

$$\Gamma_B = \frac{\Gamma_{(0,0)\rightarrow(-1,1)}\Gamma_{(-1,1)\rightarrow(0,1)}}{\Gamma_{(0,0)\rightarrow(-1,1)} + \Gamma_{(-1,1)\rightarrow(0,1)}} \tag{4.20}$$

This is again the addition of a slow rate and a fast rate, resulting in a slow net rate. In the rate calculations above, we were computing the total rate for two tunneling events in series. The two paths A and B add in parallel, so the total tunneling rate onto the trap island is the incoherent sum of the two tunneling rates

$$\Gamma_{(0,0)\rightarrow(0,1)} = \Gamma_A + \Gamma_B \tag{4.21}$$

The rate for electrons to tunnel off of the trap island, $\Gamma_{(0,1)\rightarrow(0,0)}$, is an analogous calculation. Tunneling rates for a trap circuit with island charging energy $E_{CIsl} = 2.5\ K$ and trap charging energy $E_{CTrap} = 0.7\ K$ are shown in Figure 4.8 for 50 mK and 150 mK as a function of trap gate charge, n_{gTrap}. The temperature dependence of the rates at the charge degeneracy point is shown in Figure 4.9. The effect of adding an intermediate island has the effect of significantly decreasing the first order sequential tunneling rates both as a function of gate and of temperature. Sequential tunneling rates in the trap are exponentially suppressed, and at 50 mK are effectively zero. This model is linear in the dimensionless conductance, g, which typically means that these rates will dominate over those described by the next order in perturbation theory. In this case, that is no longer true, and we must consider the next order, which is quadratic in g and involves the simultaneous tunneling of two electrons. These quantum fluctuations are the subject of the next chapter.

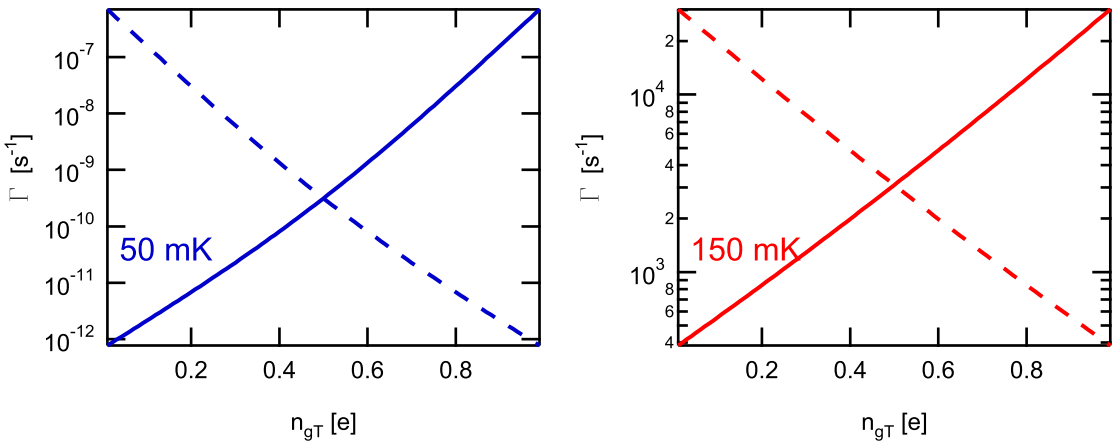

Figure 4.8: Sequential tunneling rates for a single electron trap with $g = 0.1$, $E_{CIsl} = 2.5\ K$, $E_{CTrap} = 0.7\ K$ at two temperatures, 50 mK and 150 mK. The solid line represents the $\Gamma_{(0,0)\rightarrow(0,1)}$ and the dashed line represents the reverse rate, $\Gamma_{(0,1)\rightarrow(0,0)}$. At 50 mK, there is an exponential suppression of the tunneling rates. The rates for sequential tunneling in the trap remain at levels measurable by the SET until above 150 mK, a relatively high temperature in these systems.

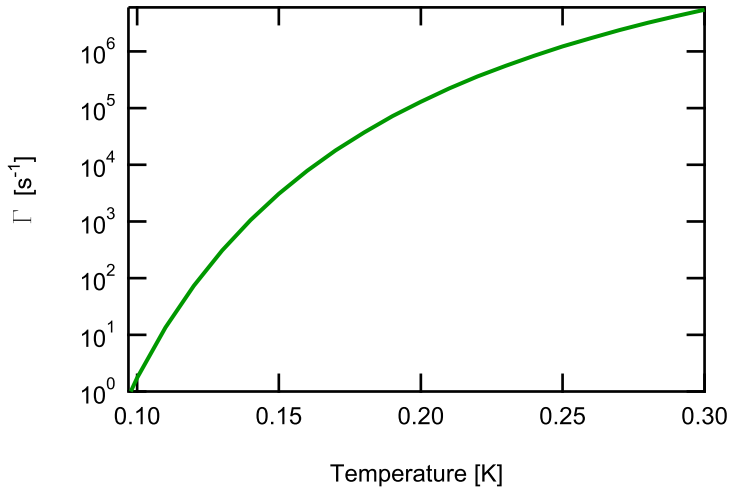

Figure 4.9: Temperature dependence of sequential tunneling rates at the charge degeneracy point for the second island in a single electron trap with $g = 0.1$, $E_{CIsl} = 2.5\ K$, $E_{CTrap} = 0.7\ K$.

Chapter 5

Cotunnelling Theory: Higher Order Quantum Events

5.1 Introduction

The orthodox theory calculations detailed in the last chapter showed that the tunneling rates in the trap become quite small at low temperatures. These rates are linear in the dimensionless conductance, g, and are typically the dominant tunneling process. When these rates are completely supressed, however, we have to go to the next order, which is outlined in this chapter.

Cotunneling, in general, is the coherent tunneling of multiple electrons through multiple junctions. It is essentially quantum in nature, as it involves the virtual occupation of intermediate, energetically forbidden states. As long as energy is conserved overall, this process enables the decay of locally stable configurations. In this chapter, I outline the calculation for the cotunneling rates in the single electron trap. In this case, the process involves the tunneling of two electrons through two junctions, creating in the process two electron-hole pairs. Unlike in orthodox theory, where the rate of electrons to tunnel onto the trap island was a sum the rates of various independent tunneling events, the total rate for cotunneling cannot be written as a sum of independent rates. Instead, the two possible paths for cotunneling onto the trap island are added coherently, and cannot be separated. Because it involves two electrons simultaneously tunneling through two junctions, the cotunneling rate is quadratic in the dimensionless conductance. The calculation presented here follows the explanation of Averin and Nazarov in Chapter 6 of the Nato series book, *Single Electron Tunneling* [Grabert1992].

Cotunneling was first described by Averin and Odintsov in 1989 [AVERIN1989], where it was

used to explain the finite current measured in the blockaded region of single electron transistors later measured by Geerligs et al. in 1990 [GEERLIGS1990] and Eiles in 1992 [Eiles1992]. It is a process in which tunneling progresses through virtual occupation of energetically forbidden intermediate states, rather than through the sequential tunneling model presented in Chapter 4. Calculations of cotunneling rates in multi-junction circuits were performed by P. Lafarge and D. Esteve in 1993 to calculate the transition between the blockaded and finite voltage states of the single electron transistor at zero temperature in a non-divergent way [Lafarge1993a]. Measurements have shown agreement with these calculations in the case of a two dimensional electron gas electrometer in the zero temperature limit [Pasquier1993]. Additionally, calculations of the cotunneling rates in multijunction pumps have been performed [Martinis1994, Keller1998, Kautz1999, Kautz2000], but comparisons with measured rates have revealed that cotunneling is not the dominant source of errors in these systems. More recently, experiments by Lehnert et al. have demonstrated measurements of the quantum fluctuations in the single electron box [Lehnert2003]. Transport in the cotunneling regime in quantum dots, which depends on the level spacing, has also been studied [Sigrist2006, Golovach2004, Wegewijs2001]. There are no known experiments, however, that probe the dynamics of the cotunneling process.

5.2 Cotunnelling in the Single Electron Trap

The cotunneling process in the single electron trap proceeds via one of two possible virtual intermediate states. These are shown in the charge configuration space picture in 5.1. This can either

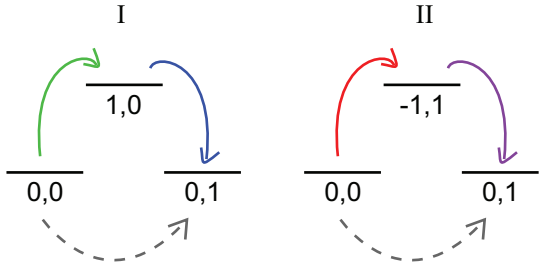

Figure 5.1: An illustration of the cotunneling process in charge configuration space. The result of the process is a real tunneling event from the (0,0) state to the (0,1) state, with a intermediate virtual excitation in either state I (1,0) or state II (-1,1).

start with a virtual tunneling event through the first junction to state (1,0) or through the second junction to state (-1,1). In the first case, labelled *I*, there is a virtual electron excitation on the

central electrode with energy ϵ_1, while in the second case, labelled II, there is a virtual hole created on the central electrode with energy ϵ_3. The final real tunneling event leaves behind either a hole or an electron with energies ϵ_2 and ϵ_4, so that the net result of the real tunneling event is an electron hole pair excitation on the central electrode and a real electron on the trap island. A diagram illustrating these two cases is shown in Figure 5.2. Because of the virtual nature of these two processes,

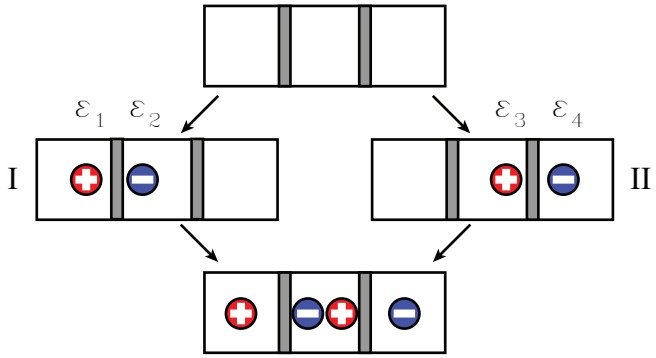

Figure 5.2: An illustration of the cotunneling process. In this diagram an electron tunnels from the reservoir onto the trap island via one of two intermediate virtual occupations of the center island. The energies indicate the final state of the cotunneling process. In the first path, I, there is a virtual tunneling event across the first junction, creating a virtual electron on the intermediate island and leaving a hole behind. In the second process, the first tunneling event is across the second junction, creating a virtual hole excitation on the middle electrode, leaving an electron on the trap island. The final process is the second tunneling event, which ends with a real electron on the trap island.

the two paths are indistinguishable and cannot be separated. We can write down an expression for the tunneling rate using Fermi's Golden rule. In this case we will have the matrix elements for tunneling through each junction as well as an energy denominator due to the fact that these are virtual transitions. These elements are then multiplied by the probability to find an electron state ϵ_1 and an unoccupied state ϵ_2. These terms are then multiplied by equivalent terms for the alternate process. We then integrate over all possible intermediate energies, resulting in the expression

$$\gamma = \frac{\hbar}{2\pi e^4 R_{t1} R_{t2}} \int_{-\infty}^{\infty} d\epsilon_1 d\epsilon_2 d\epsilon_3 d\epsilon_4 f(\epsilon_1)(1-f(\epsilon_2))f(\epsilon_3)(1-f(\epsilon_4)) \tag{5.1}$$
$$\times \left(\frac{1}{\epsilon_1 + \epsilon_2 + E_I} + \frac{1}{\epsilon_3 + \epsilon_4 + E_{II}} \right)^2 \delta(\Delta E - (\epsilon_1 + \epsilon_2 + \epsilon_3 + \epsilon_4))$$

where

$$E_I = E(1,0) - E(0,0) \tag{5.2}$$

$$E_{II} = E(-1,1) - E(0,0) \tag{5.3}$$

$$\Delta E = E(0,1) - E(0,0) \tag{5.4}$$

E_I and E_{II} are the energy costs for each of the intermediate states, and ΔE is the total energy difference between the initial and final states. The total electrostatic energy of the trap is $E(n_{Isl}, n_{Trap})$, which was defined in Chapter 4. At zero temperature, this integral can be solved explicitly and the tunneling rate is given by

$$\gamma = \frac{g^2}{4\pi^2 h}\left[\left(1+\frac{2}{\Delta E}\frac{E_I E_{II}}{E_I+E_{II}+\Delta E}\right)\left(\sum_{i=1,2} ln(1+\Delta E/E_i)\right)-2\right]\Delta E \tag{5.5}$$

which is plotted as a function of trap gate in Figure 5.3. The cotunneling process will only occur if

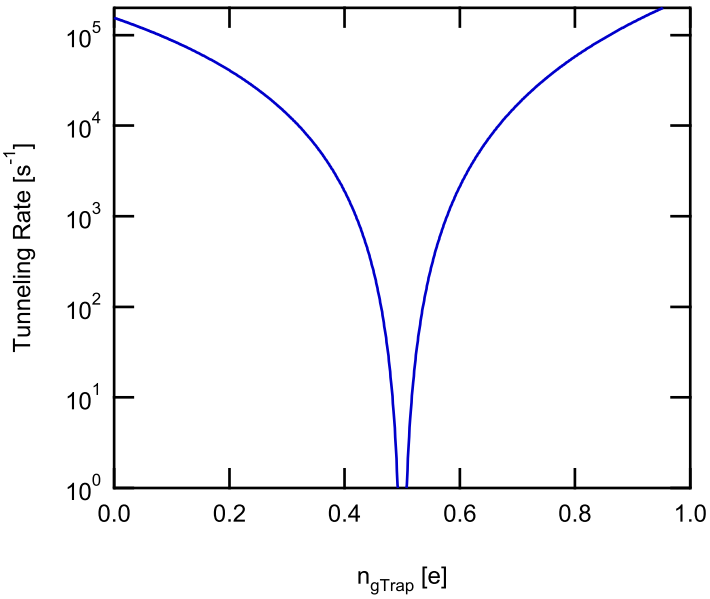

Figure 5.3: Cotunneling rates for the trap at zero temperature. The tunneling rates at zero temperature diverge at the charge degeneracy point where the energy difference between the two charge states goes to zero. If the total energy difference between the initial and final state is less than zero, the process will not proceed. This means that only the rate to tunnel from the excited state to the ground state is defined at zero temperature. This would also be true for orthodox theory.

there is an overall energy gain. At zero temperature, there is no thermal activation of cotunneling, and there will rate is only defined for tunneling from the excited state to the ground state. At energy degeneracy, or for negative energy difference, there is no rate defined for cotunneling, and the rates diverge to zero.

At finite temperatures, we must work to simplify the integral expression and integrate it numerically. Making use of the relation

$$\int_{-\infty}^{\infty} f(E)(1-f(E+x))dE = \frac{x}{1-e^{-\beta x}} \tag{5.6}$$

we can rewrite this expression as

$$\gamma = \frac{\hbar}{2\pi e^4 R_{t1} R_{t2}} \int_{-\infty}^{\infty} \frac{E}{1-\exp(-\beta E)} \frac{E'}{1-\exp(-\beta E')} \times \left(\frac{1}{E+E_I} + \frac{1}{E'+E_{II}} \right)^2 \delta(\Delta E - E' - E) dE dE' \tag{5.7}$$

where E and E' are the energies of the electron-hole pairs created in this process. The energy denominator contains a real divergence for certain high energies of the intermediate states. We can remove this divergence by taking into account the finite lifetimes of the intermediate states. The correct way to add these in would be to go to higher orders in perturbation theory, but to first order, I will calculate these using the sequential tunneling model (see Chapter 4), to find the tunneling rates out of each virtual intermediate state. These rates are given for each process as Γ_1 and Γ_2 where

$$\Gamma_1 = \Gamma_{(1,0)\to(0,0)} + \Gamma_{(1,0)\to(0,1)} \tag{5.8}$$

$$\Gamma_2 = \Gamma_{(-1,1)\to(0,0)} + \Gamma_{(-1,1)\to(0,1)} \tag{5.9}$$

and Γ is just the equation for first order, sequential tunneling. Adding in the lifetimes of the intermediate states changes the energy denominator term in the following way[1]

$$\frac{1}{E+EI} \to \frac{E+E_I}{(E+E_I)^2+(\hbar\Gamma_1)^2} \tag{5.10}$$

$$\frac{1}{E'+EII} \to \frac{E'+E_{II}}{(E'+E_{II})^2+(\hbar\Gamma_2)^2} \tag{5.11}$$

The final integral expression we are left with is then

$$\gamma = \frac{\hbar}{2\pi e^4 R_{t1} R_{t2}} \int_{-\infty}^{\infty} \frac{E}{1-\exp(-\beta E)} \frac{E'}{1-\exp(-\beta E')} \times \left(\frac{E+E_I}{(E+E_I)^2+(\hbar\Gamma_1)^2} + \frac{E'+E_{II}}{(E'+E_{II})^2+(\hbar\Gamma_2)^2} \right)^2 \times \delta(\Delta E - E' - E) dE dE' \tag{5.12}$$

This expression is plotted as a function of trap gate charge at 50 mK in Figure 5.4 and as a function of temperature in Figure 5.5 using the expected parameters for the devices measured for this thesis. The total rate calculated using this method is not highly dependent on the exact value for the lifetimes of the intermediate states. As long as the inverse lifetimes are small enough, they do not affect the final answer as shown in Figure 5.6, where the tunneling rate in the trap (calculated at a

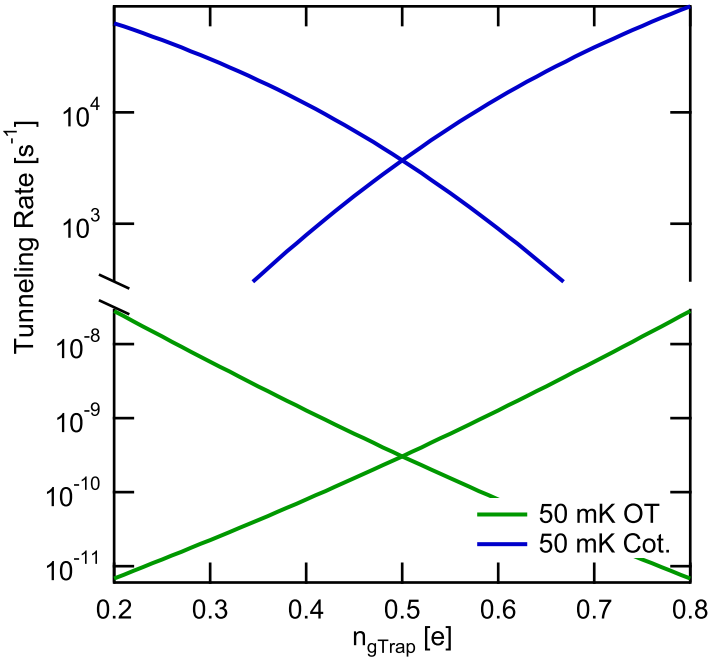

Figure 5.4: The top curve shows the cotunneling rates for the trap at as a function of gate voltage for a device at 50 mK. These calculations are for a trap with charging energy 0.7 K, island charging energy of 2.5 K, and dimensionless conductance g=0.1.

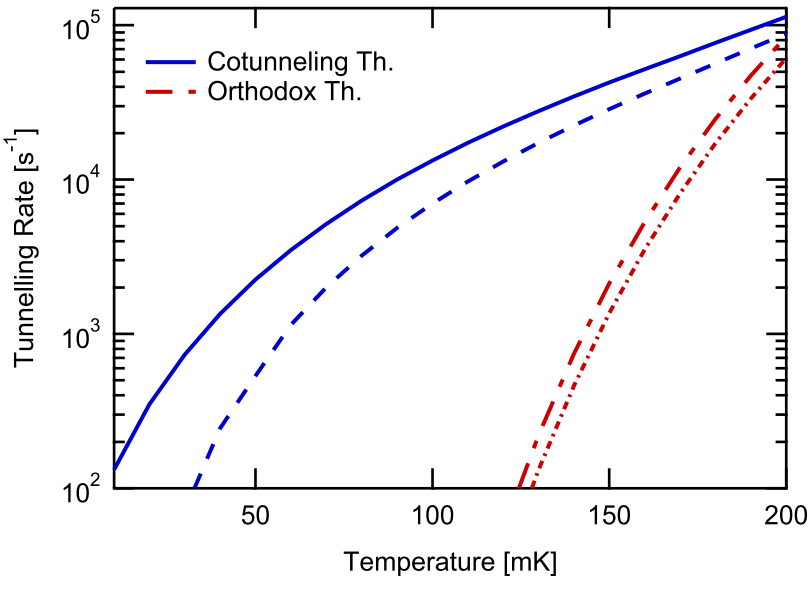

Figure 5.5: The top curve shows the cotunneling rates for the trap at as a function of temperature. These predictions are for an island bias of $n_{gIsl} = 0$ and trap bias of $n_{gTrap} = 0.55$ for a trap with charging energy 0.7 K, island charging energy of 2.5 K, and dimensionless conductance g=0.1. Also plotted are the Orthodox theory rates for the same bias conditions.

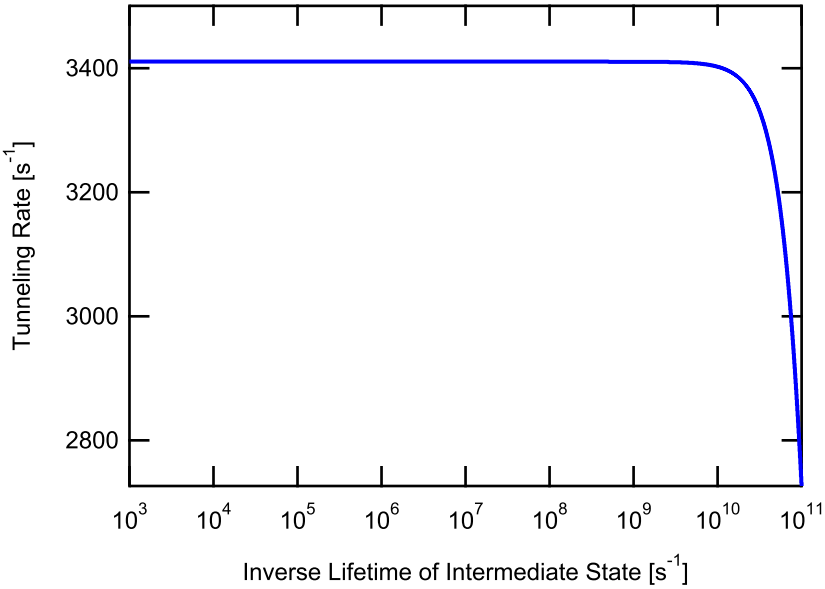

Figure 5.6: Tunneling rate of the trap calculated at the charge degeneracy point at 50 mK as a function of the inverse lifetime of the intermediate state. The divergence in the cotunneling calculation is removed by considering the finite lifetime of the intermediate state, which comes into the energy denominator as $\hbar$ times the rate to tunnel out of the intermediate state. The equations are not dependent on the value of this quantity until it starts to dominate the energy denominator.

particular gate voltage) is plotted as a function of this inverse lifetime. I will present measurements and results from two specific devices, called A and B in Chapter 8, and the parameters used for cotunneling rate curves correspond to these two devices.

5.3 Incorporating the Backaction of the SET

The backaction of the SET also contributes to the shape of the rate curves. For the two devices that have been measured, the forward and reverse couplings for each device to the SET are shown in table 5.1. The forward coupling corresponds to the strength with which the SET measures the trap island, or what percentage of each trap electron is coupled to the SET island, and is given by $C_C/C_{\Sigma Trap}$. The reverse coupling is the strength with which the trap measures the SET island, or how much the potential of the trap is shifted with an additional electron added to the SET island. The reverse coupling is given by $C_C/C_{\Sigma SET}$. Device A was not coupled strongly enough to the SET to allow for time resolved measurements of single tunneling events. Device B was much more strongly coupled

[1]The calculation presented here is a result of private conversations with Aashish Clerk at McGill. Similar methods for removing this divergence are presented in Lafarge et al. [Lafarge1993a].

	$\kappa_{Trap} = C_C/C_{\Sigma Trap}$	$\kappa_{SET} = C_C/C_{\Sigma SET}$
Device A	2.3%	10%
Device B	10.3%	23%

Table 5.1: Forward and reverse coupling for the two devices measured in this thesis. The size of the signal is determined by κ_{Trap}, which was much larger in device B than in device A. This comes at the price of the reverse coupling, which is also much higher in device B than in device A. The reverse coupling is the percentage on electron on the SET island that couples to the trap island.

to the SET, but this comes at a price of a much higher reverse coupling, and more backaction from the SET. As long as the tunneling rates of the electrons on and off of the SET island are much faster than the tunneling rates on the trap, we can just use a simple weighted average of the trap tunneling rates with the SET having 0 and 1 electrons. The change in charge of the SET island by one electron acts as an effective gate bias for the trap island, shifting the rate curves slightly with respect to the n_{gTrap} axis. The rate of tunneling on and off of the trap island is calculated for the two possible charge states of the SET. We then add them together, weighting each rate by the probability of the SET to be in that particular charge state, given the bias conditions of the SET and the initial charge state of the trap. The total tunneling rate of the trap between charge states (0,0) and (0,1) is

$$\Gamma_{(0,0)\rightarrow(0,1)} = \Gamma_{(0,0)\rightarrow(0,1)}|_{n_{SET}=0} P_0 + \Gamma_{(0,0)\rightarrow(0,1)}|_{n_{SET}=1} P_1 \tag{5.13}$$

The first term is the tunneling rate from (0,0) to (0,1) given that the charge on the SET is 0, multiplied by the probability that the SET island has 0 excess electrons. The second term is calculated given that the SET is in the 1 state. The reverse rate is given by an analogous equation.

The probabilities to find the SET in the 0 or 1 states are calculated using the sequential tunneling model to calculate the tunneling rate between the two states, 0 and 1. The probabilities are then given by detailed balance

$$P_0 = \frac{\Gamma_{1\rightarrow 0}}{\Gamma_{0\rightarrow 1} + \Gamma_{1\rightarrow 0}} \tag{5.14}$$

$$P_1 = \frac{\Gamma_{0\rightarrow 1}}{\Gamma_{0\rightarrow 1} + \Gamma_{1\rightarrow 0}} \tag{5.15}$$

We also must account for the RF-bias of the SET with a maximum voltage V_{max} centered around $V_{ds} = 0$, so we calculate these probabilities as a function of voltage, e.g. $P_0(V)$, multiply by the probability of that voltage $P(V)$, and integrate over the range of voltages. This gives the total

probabilities for the 0 and 1 states

$$P_0 = \int_{-V_{max}}^{V_{max}} P_0(V)P(V) \tag{5.16}$$

$$P_0 = \int_{-V_{max}}^{V_{max}} P_1(V)P(V) \tag{5.17}$$

where

$$P(V) = \frac{1}{\pi}\frac{1}{\sqrt{V_{max}^2 - V^2}} \tag{5.18}$$

The full electrostatic energy equation including the SET as well as the trap circuit is given by

$$\begin{aligned} E &= E_{CTrap}(n_{Trap} - n_{gTrap})^2 + E_{CIsl}(n_{Isl} - n_{gIsl})^2 \\ &+ E_{CSET}(n_{SET} - n_{gSET} - C_{jSET}V_{ds}/e)^2 \\ &+ 2E_{CoupTI}(n_{Trap} - n_{gTrap})(n_{Isl} - n_{gIsl}) \\ &+ 2E_{CoupST}(n_{Trap} - n_{gTrap})(n_{SET} - n_{gSET} - C_{jSET}V_{ds}/e) \\ &- peV \end{aligned} \tag{5.19}$$

where C_{jSET} is the junction capacitance of the SET, E_{CoupTI} is the coupling energy between the trap and the island, and E_{CoupST} is the coupling energy between the SET and the trap. The last term, $-peV$, corresponds to the work done by the voltage source for p electrons to tunnel through the SET circuit. All of the other terms were introduced in Chapter 4.

The cotunneling rates including the backaction are plotted as a function of trap gate charge in Figure 5.7 and as a function of temperature in Figure 5.8. The original calculations, not including the backaction, are shown for comparison.

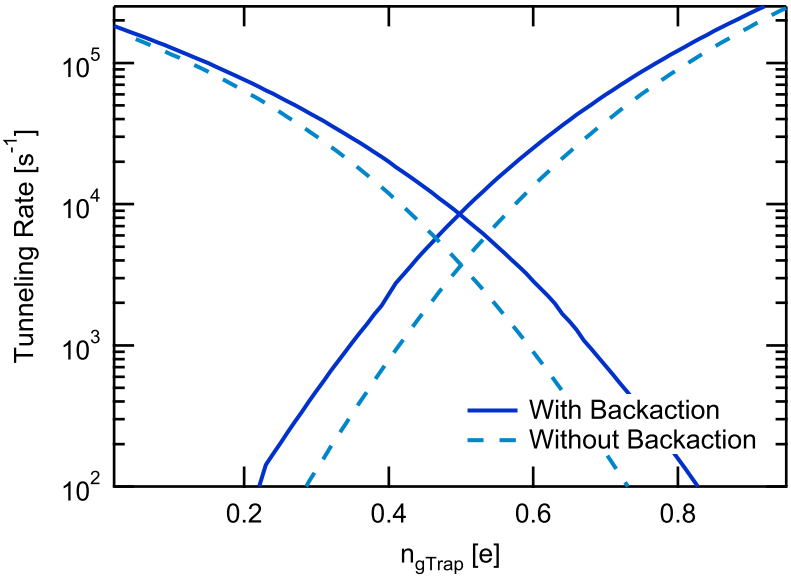

Figure 5.7: Cotunneling rates for the trap with and without the backaction of the SET as a function of trap gate. These predictions are for an island bias of $n_{gIsl} = 0$ and trap bias of $n_{gTrap} = 0.55$ for a trap with charging energy 0.7 K, island charging energy of 2.5 K, and dimensionless conductance g=0.1.

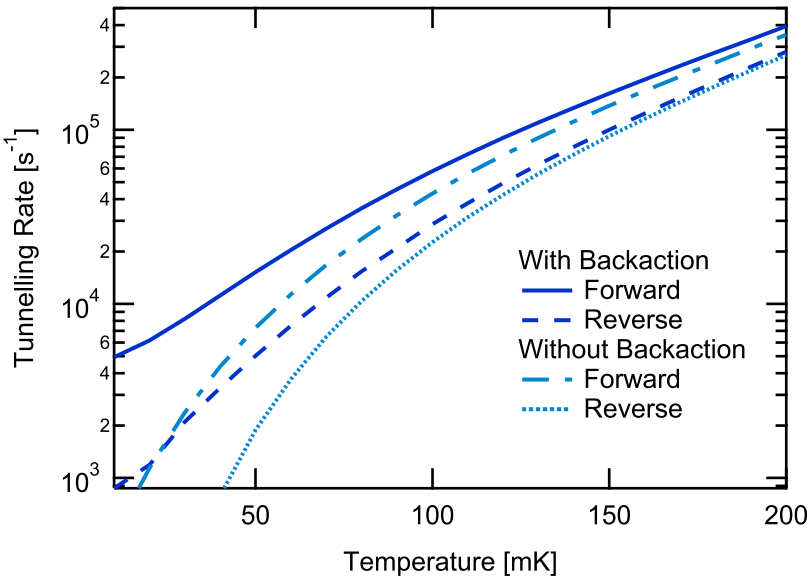

Figure 5.8: Cotunneling rates for the trap with and without the backaction of the SET as a function of temperature. These curves are for a trap gate bias slightly away from charge degeneracy at $n_{gTrap} = 0.55$ for a trap with charging energy 0.7 K, island charging energy of 2.5 K, and dimensionless conductance g=0.1.

Chapter 6

Circuit Design and Fabrication

6.1 Overview

The samples used in the experiments presented in this thesis are created using standard techniques for electron beam lithography and double angle aluminum evaporation [Dolan1977]. The majority of this chapter will focus on the elements of the process that proved to be important for fabricating my samples in particular, but I will outline the entire process. I will start by discussing the specific requirements for this experiment as well as useful design considerations. Then I will present my fabrication process. The important elements for this process were careful circuit design, as the experiment requires somewhat specific ratios for the capacitances in the problem as well as a stable method for fabricating the small junctions I required. The specifics of the recipes are detailed in appendix A.

6.2 Design Considerations

The tunneling rates in the trap experiment depend on energy differences between charge states and the detection sensitivity depends on the SET parameters as well as the coupling between the trap and SET islands. Many of the experiments rely on the independent biasing of the islands with the gate electrodes. This is difficult to fabricate in two dimensional metallic circuits, but, as explained in Chapter 3 in the example of the charge measurement of the box using the SET, this can be accomplished with various gate sweeps to counter the unintentional effects of gates. This process becomes more complicated as the number of islands increase, because the size of the capacitance matrix which must be solved for and diagonalized increases as the square of the number of islands. The degree to which the islands can be biased independently of each other depends on

all of the parasitic, or unwanted, capacitances in the problem. All of these depend on the physical characteristics of the circuit. Here I will go into detail on the specific requirements, in order of importance to the experiment while keeping in mind the feasibility in terms of the fabrication. The discussion will be qualitative, as there are trade-offs between the different priorities, and it comes down to judgement calls and preferences for operating the experiment. The process of fabricating the small junctions required by the experiment is an inexact science which I try to parameterize as specifically and stably as possible.

The most important design parameter is the ratio of the charging energy of the island, E_{CIsl}, to that of the trap, E_{CTrap}. In order to achieve the energy level diagram shown in Figure 2.4b, the island charging energy must approximately double that of the trap. This condition produces the intermediate, higher energy, barrier state over which the electron must go to make it to the trap island. The overall scale of the tunneling rates is also set in part by the charging energy of the intermediate island, which sets the height of the energetically forbidden intermediate charge state, so it is beneficial to make this value reasonably large. The island charging energy is determined primarily by the size of the junctions with the size of the island and the gate capacitor contributing to a lesser extent, so we make the junctions as small as can be fabricated reliably.

The first test of a fabrication process in the case of the SET is to probe the junctions at room temperature. The resistance scales with the area of the junctions and the thickness of the barrier, so an estimate can be made of the junction size from this test. Unlike a SET, there is no drain-source current in the trap that can be probed at room temperature to determine the viability of the junctions. These small junctions can also be damaged in the process of imaging with the scanning electron microscope (SEM), so when the sample is cooled down in the dilution refrigerator, it is done so blindly. For this reason, the trap island and junctions are made to be very similar to those of the SET which can be probed at room temperature. Typically, if the fabrication process went well for SET junctions it will have also gone well for the trap junctions. For the same deposition parameters, smaller junctions have higher resistance which helps to lower the tunneling rates. The sequential tunneling rates go as g while the cotunneling rates go as g^2, so this is an important parameter that sets the overall scale of the rates. Typical current densities that are achieved by this fabrication process approximately $25 - 30\ A/cm^2$.

The considerations for the SET design are analogous to those for the island in that we also want to have small junctions, both to make the SET similar to the island for the reasons described above,

and because the gain of the SET used as an electrometer improves with the SET charging energy. Optimally, the SET would have a high charging energy with low ($\sim 50 - 100\ k\Omega$) series resistance of the tunnel junctions. In practice, we have not achieved this with our deposition system, and the two junctions that are $50 \times 50\ nm$ typically have a series resistance of ($\sim 500\ k\Omega$). Such a high resistance is difficult to match to the 50 Ω cabling at the center frequency of our amplifiers, which will be discussed in more detail in the next chapter. To achieve a balance between charging energy and junction resistance, the SET junctions are fabricated to be just slightly larger than those for the island, and I try to make something that is $\sim 50 \times 70 - 100\ nm$, with a series resistance that is slightly lower.

For the trap design, I require $E_{CTrap} < E_{CIsl}/2$. The trap only has one junction, so to increase the total capacitance the trap island must be much larger. Two other priorities also increase the capacitance of the trap. The first is to have high coupling between the trap and the SET and the second is that the gates are coupled to their corresponding islands as strongly as possible while minimizing the capacitance to neighboring islands. Strong coupling to both the trap gate and the SET will increase the total capacitance of the trap.

6.3 Modelling Capacitances

To achieve the desired circuit that was outlined in the last section, it is crucial that we are able to simulate the coupling between the metallic leads and islands in the circuit. Fabrication of nanoscale circuits is time consuming and constrained by other users. If the non-junction related capacitances can be carefully designed in software, the only elements to be tuned in the fabrication process are the junctions themselves.

In order to effectively design a set of capacitances in a 2-D thin film circuit it is useful to develop an intuition for how these circuits behave. The circuits themselves are 2-D Aluminum thin films, but all of the field lines are in 3-D. This necessitates a 3-D field simulator and makes it impossible to shield different sections of metal from each other by depositing more metal in the same plane. The other limitation of the lithography process is the substrate we are using. In order to be able to probe the devices (the SET in particular) at room temperature, we use an insulating layer on top of the silicon as it is conducting at room temperature. In our case this is a thin ($200 - 400\ nm$) layer of SiO_2. The effect of the bilayer substrate, with Si having $\epsilon \sim 12$ and SiO_2 with $\epsilon \sim 3$, is that the metals close together, that we want to couple strongly, have a relatively smaller coupling with

respect to those that are farther away than they would on a uniform substrate.

The software used for these simulations is the Maxwell Electromagnetic Field Simulator. The simulation process is to import the proposed lithography pattern, assign each element a material, and each metallic element a voltage. This program uses finite element analysis to solve for the fields and can also be set to solve for the capacitance matrix. I have been fairly successful using this method to design my capacitances, as shown in table 6.1, which shows the simulated values of a particular design along with experimentally determined capacitances. It is not useful to try to simulate the tunnel junctions with this model so these capacitances are added back in by hand.

Capacitor	Measured Value [aF]	Simulated Value [aF]	Error %
SG-S	32.3	24	-26
SG-T	100.8	100	-0.8
SG-I	*	7.5	-
TG-S	26	17	-35
TG-T	383	400	4
TG-I	24	19	-21
IG-S	11.3	9.5	-16
IG-T	258	178	-31
IG-I	33	45	36

Table 6.1: Simulated and measured values for capacitances for one device measured for this thesis. The labelling notation for the capacitors is gate-island, e.g. SG-S is the capacitance from the SET gate to the SET island. The * indicates quantities that are too small to measure. The third column lists the error in the simulation as a percentage of the measured value. It is not surprising that many of the values measured, especially capacitances of metals which are physically far from each other are simulated to be too small because only a small area of the circuit is simulated.

Figure 6.1 shows a completed design for device A, and Figure 6.2 shows the design for device B. In both designs, the island is designed to be as similar to the island of the SET and the island gate capacitor wraps around it to increase direct coupling. The trap island is made much larger than the other two islands to reduce the trap charging energy through increased capacitance to ground as well nearby electrodes. Device A had a much smaller coupling of the trap island to the SET island. This coupling of the trap to the SET is strengthened in device B by wrapping the trap island around the SET island. Similarly, a finger capacitor gives a high coupling between the trap gate and the trap island. In general, the capacitances increase with the longest linear dimension, which explains the particular shapes I have chosen. The strong trap gate capacitor helps to separate the gates by coupling the trap gate 50 times more strongly to the trap island than to the island. In the experiment, this means that the island gate will not need to be counter-swept for small changes in

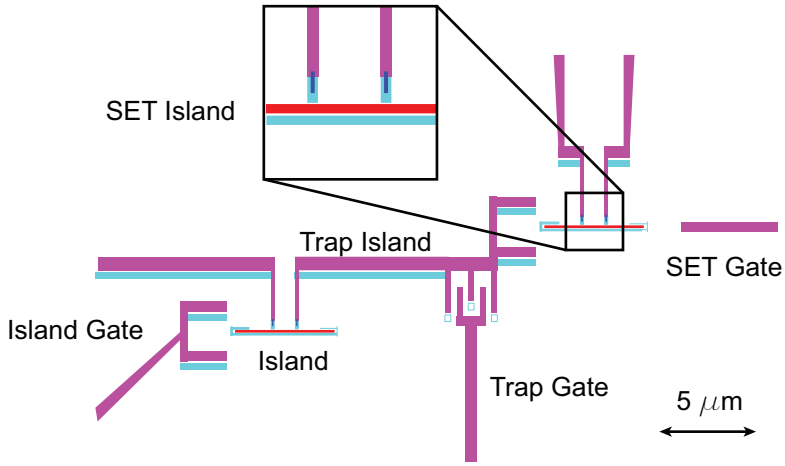

Figure 6.1: Detailed view of the active center section of the circuit diagram for device A. The magenta areas are the larger features of this section of the circuit and are given a constant dose. Red elements are the SET island and the barrier island, and the blue elements are the fingers. Cyan indicates the areas where undercut dose is applied. The doses red, blue, and cyan elements are found by the dose array that is outlined in the final section of this chapter.

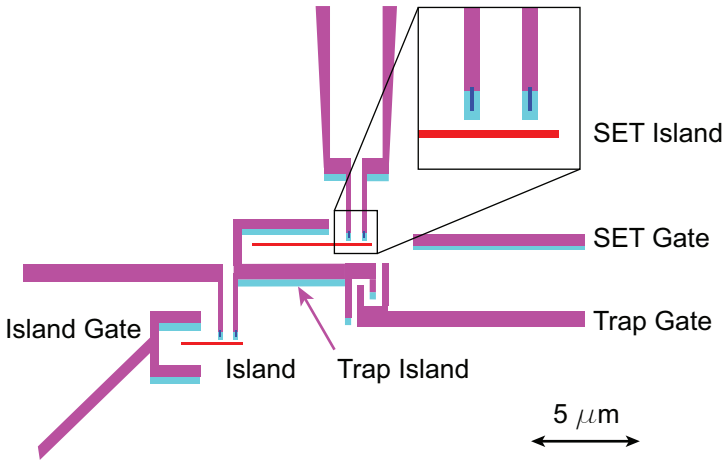

Figure 6.2: Detailed view of the active center section of the circuit diagram. The magenta areas are the larger features of this section of the circuit and are given a constant dose. Red elements are the SET island and the barrier island, and the blue elements are the fingers. Cyan indicates the areas where undercut dose is applied. The doses red, blue, and cyan elements are found by the dose array that is outlined in the final section of this chapter.

trap gate charge, which greatly simplifies the operation of the experiment. I have also positioned the island far from the SET island both to separate the gates and to try to shield the island from the SET island. The measured signal on the SET is then almost entirely due to electrons tunneling on and off the trap island, which is coupled 100 times more strongly than the intermediate island to the SET island in device B. The final design complete with bonding pads and connecting wires is shown in Figure 6.3.

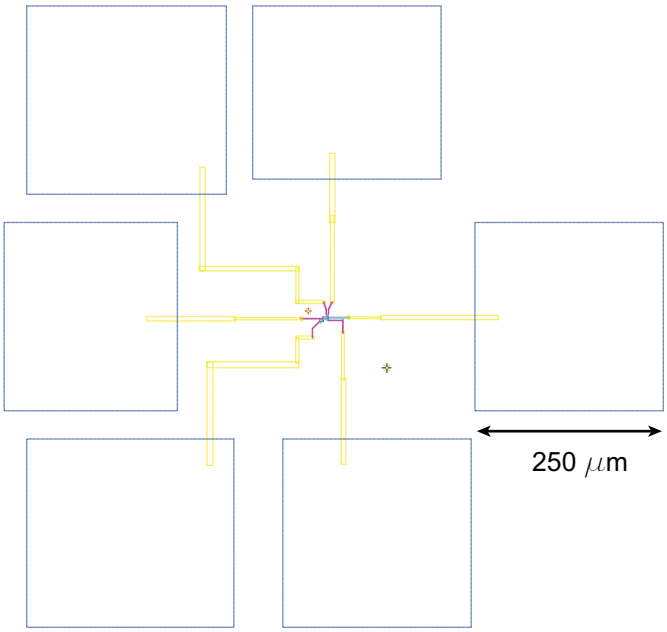

Figure 6.3: Circuit layout for for the single electron trap. The yellow lines are the wiring from the central area of the circuit out to the large blue squares which are the pads for the wire bonds.

6.4 Fabrication Using Electron Beam Lithography

Sample fabrication follows a standard technique of electron beam (or e-beam) lithography, as illustrated in the cartoon in Figure 6.4. Our particular technique is to expose a positive bilayer resist with a 30 keV electron beam to create a mask of the pattern shown in Figure 6.3. We then create the junctions using the double angle evaporation, or Dolan bridge technique, which makes use of suspended structures in the top layer of the resist. Here, I will outline each step of the process of the fabrication, and a detailed recipe can be found in the appendix.

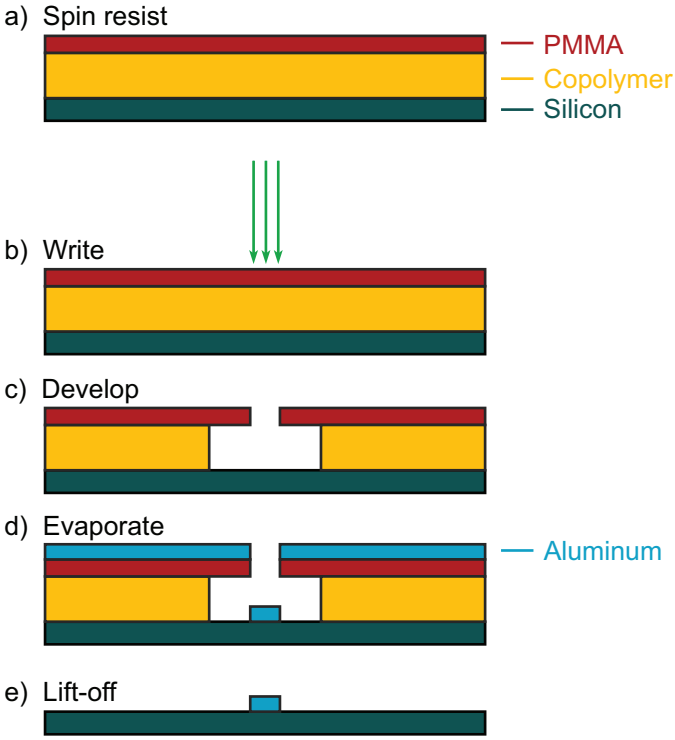

Figure 6.4: Cartoon diagram of the electron beam lithography fabrication process. a) The first step in the process is to spin a bilayer of resist on a two inch silicon wafer. This wafer is then diced into smaller chips. b) The second step is to write the pattern by exposing the resist with 30 keV electrons in a SEM. c) The exposed regions of the resist are removed during the development process. d) Metal is evaporated using a double angle technique with an oxidation step in between the two layers. Only the first depositions step is shown here. e) The final step in the process is to remove the remaining resist from the silicon chip, leaving behind only the aluminum that was deposited directly onto the silicon.

6.4.1 Wafer Preparation

The junction fabrication technique requires a bilayer resist shown in Figure 6.4a. The areas of the resist exposed to the e-beam will be removed upon development, and the differing sensitivities to exposure of the two layers allow us to achieve an undercut in the bottom layer, as shown in Figure 6.4c. We start with a clean two inch silicon wafer onto which a native oxide has already been grown by wet oxidation of the silicon at 1000 C for about one hour. The wafer is rinsed in acetone and methanol and spun with MicroChem MMA(8.5) MAA EL12 [1] to a thickness of about 550 nm. The MAA first layer acts as a copolymer for the top layer. The wafer is then baked on a hotplate fitted with a flat aluminum plate to ensure temperature uniformity across the wafer at 170 C for 5 minutes. It is cooled on a room temperature aluminum plate for 60 s and the second layer of resist, MicroChem 950K PMMA A3[2], is spun to a thickness of about 100 nm and then baked at the same temperature for 30 minutes and cooled for 60 s. The wafer is diced into chips each approximately 1 cm^2, each of which is patterened separately in the SEM. This yields many chips with which to perfect the fabrication process, with a high uniformity in resist thickness across the samples.

6.4.2 Electron Beam Lithography

Electron beam lithography is performed with an FEI Sirion scanning electron microscope model XL 30 outfitted with the Nabity Pattern Generation System (NPGS). This microscope has a minimum viewing resolution of 4 nm, and lines can be etched reliably in a bilayer resist as described above down to about 40 nm. The Nabity system allows us to write a script for the microscope setting the patterns to be used, writing order, and exposure doses of each design element. Because the small junctions are near the performance limits of the microscope and have a high degree ($\sim$ 100%) of variability, I write as many samples on a chip as possible to have the highest likelihood of having a sample that meets the needs of the experiment. The exposure is done using an accelerating voltage for the electrons of 30 keV which we have found allows us the most control in writing the very narrow lines needed for constructing the junctions. The pattern written is shown in Figure 6.3 with a higher magnification view in Figure 6.2. The colors in the diagram indicate the groupings that are exposed with the same dose. The magenta areas of the circuit have a fixed dose of 350 $\mu C/cm^2$, and the red, blue, and cyan areas are tuned by writing a large scale dose array as discussed later in this

[1] Methyl methacrylate (MMA) 8.5% by weight in methacrylic acid (MAA) in a 12% by weight solution in ethyl lactate (EL)

[2] 950,000 Dalton Poly-methyl methacrylate (PMMA) in a 3% by weight solution in Anisole (A)

chapter. In this diagram, the magenta, red, and blue sections will be etched through both layers of resist, while the cyan is written at a much lower dose ($\sim 60\ \mu C/cm^2$), only exposing the lower layer. There is a natural undercut in the lower layer because it is more sensitive to the exposure, and the cyan areas are written to allow more precise control over the lower layer. The need for this will become more apparent in the discussion of the double angle evaporation.

After writing, the chip is developed in a solution of MIBK:IPA 1:3 [3] kept at 25 C in a heated water bath to ensure temperature consistency between runs. A photograph taken in an optical microscope of the resist after development is shown in Figure 6.5.

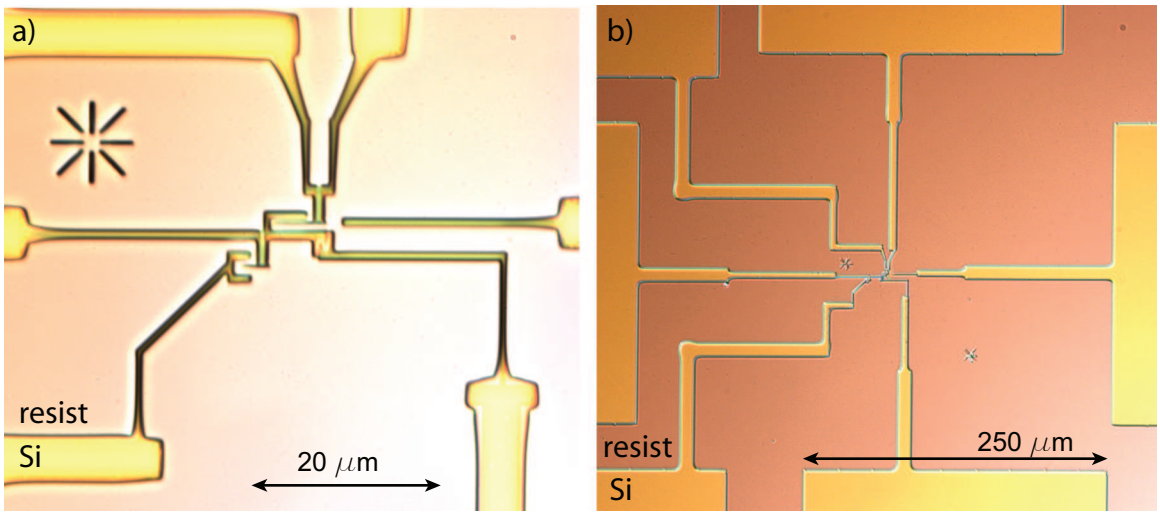

Figure 6.5: Image taken in the optical microscope of the resist after exposure and development. a) Detail of the circuit. b) Wider view showing connections to bond pads.

6.4.3 Aluminum Evaporation

The most important part of the aluminum evaporation is the junction creation, using the Dolan bridge technique [Dolan1977], [Niemeyer1974]. The advantage of this technique is that our junctions are self aligned and can be kept under vacuum for the entire process. We are starting with a bilayer that has strategically placed areas of PMMA that are completely suspended above the silicon. Figure 6.6a shows the top view of this structure with the dark red indicating the PMMA/copolymer bilayer and the lighter areas indicating the suspended structures. A side profile of this structure is shown in Figure 6.6b. The sample is loaded in the Plassys e-beam evaporator and the load lock and chamber are pumped to a base pressure of $3 \times 10^{-7}\ Torr$. A short titanium evaporation (with a shutter

[3] Methyl isobutyl ketone (MIBK) and Isopropilic alcohol (IPA) in a 1:3 ratio in volume

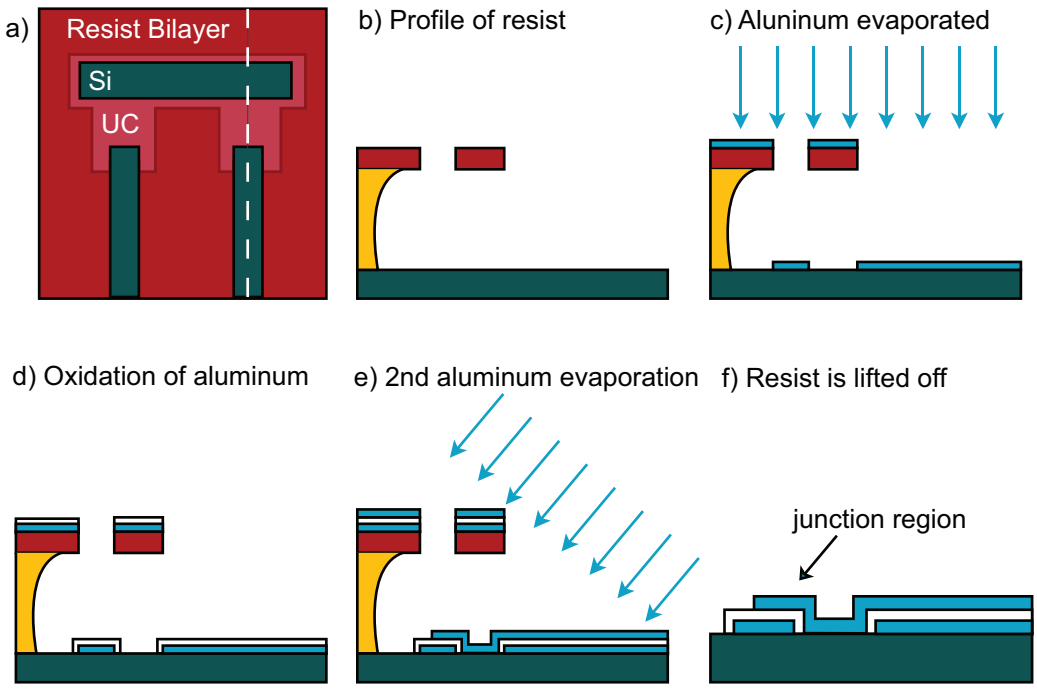

Figure 6.6: a) A pattern exposed in a bilayer resist. This view is looking down from the top through the resist onto the silicon below. The bilayer exists in the red region while there is only a single layer in the lighter regions. b) A side profile view along the white dotted line in the first frame. As is visible here, there is a single layer between the finger and the island that is completely suspended. c) Aluminum is evaporated at 0 degrees through the resist mask. d) The first layer of aluminum is oxidized. e) The second layer of aluminum is evaporated at an angle so that the fingers extend onto the island, forming an overlap region which is the tunnel junction.

shielding the sample) lowers the pressure to 1×10^{-7} *Torr*. The shutter is moved and a 35 nm layer of aluminum is deposited straight through the mask as shown in 6.6c. A SEM image taken just after this step is shown in Figure 6.7a. In this image, you can see the top bright areas of the mask,

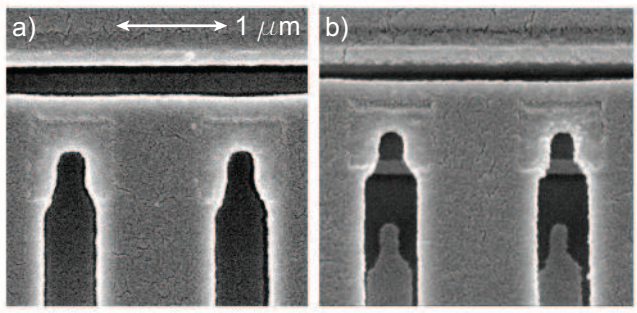

Figure 6.7: SEM micrograph midway through the fabrication process. a) 10 nm of aluminum deposited on resist at 0 degrees, viewed directly from above. The bright edges outline the holes in the mask, and everything visible is aluminum. b) Same chip, viewed at 35 degrees. Here we are looking through the resist mask and can see where the second layer would have landed. To accentuate the image, the viewing angle is larger than the deposition angle.

and looking inside the trenches, you can see a layer of aluminum. The aluminum layer inside the trench is more visible in Figure 6.7b, which is tilted slightly. Figure 6.8 shows another SEM image taken with a wider zoom in which the PMMA/copolymer profile is also visible. The chamber is

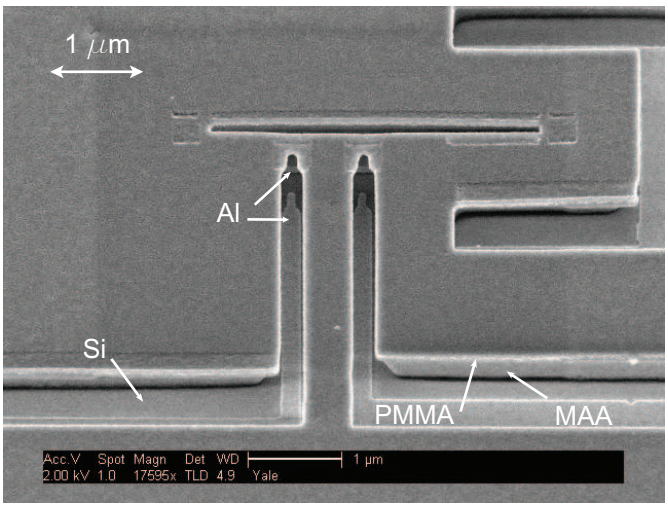

Figure 6.8: SEM micrograph midway through the fabrication process. Aluminum has been deposited at 0 degrees. The sample is tilted at about 40 degrees looking through the resist mask where the second layer of Aluminum would be deposited. In the lower part of the image, the MAA/PMMA resist profile is visible.

filled with an Ar:O_2 (85% : 15%) mixture for 12 minutes at 3 Torr and an oxide is grown on the first

aluminum layer. The oxidation is a very delicate step in this process, and the addition of the argon to the oxygen serves to raise the total pressure in the chamber, reducing the outgassing from the resist bilayer. Without breaking vacuum, the sample is tilted by approximately 30°, and the second layer of aluminum is deposited on the substrate. The second, shadow image of the fingers now is shifted to make contact with the island, making an Al:Al0_x:Al tunnel junction at the overlap. The circuit has been designed to cause the shadow island to be deposited onto the resist wall so that it does not appear in the final circuit. The deposition of the second layer is more clearly shown in Figure 6.7b. The sample is tilted at 35° to show the destination of the second layer of aluminum. The actual deposition angle would expose just the edge of the island to make the overlap as small as possible. This image is taken with a steeper angle to give a more clear image of the island. The chip is removed from the deposition system, submerged in a hot ($\sim 55\ C$ with the hot plate set to 70 C) acetone bath for 15 minutes, and sonicated for 30 seconds. A SEM micrograph of the junctions formed on the island is shown in Figure 6.9, and Figure 6.10 shows the a micrograph of the final

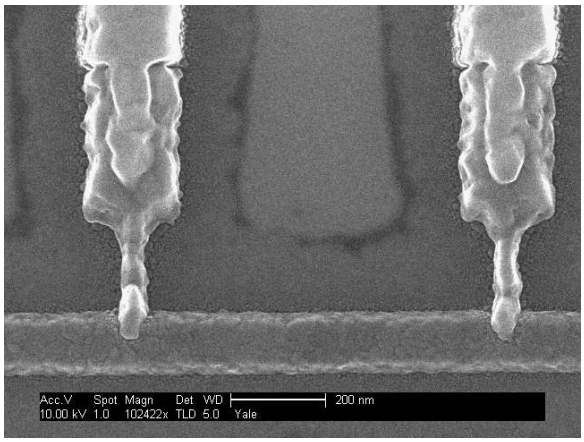

Figure 6.9: Close up image of the island junctions. Tunnel junctions are formed by the overlap of the fingers (vertical bars) and the island (horizontal bar).

circuit for device A, and Figure 6.11 shows the final circuit design for device B. As I said at the beginning of this chapter, I never view the devices in the SEM before they are measured to avoid damaging the small junctions[4]. For many reasons, none of which related to the circuit design or the junctions themselves, I had a much tougher time fabricating circuits reliably during the time when I fabricated the second device presented here. The actual circuit, viewed after the measurement

[4]I have not found viewing to be a problem with larger junctions (50 x 100 nm^2), but I have found that the small junctions in these circuits can be damaged in the SEM.

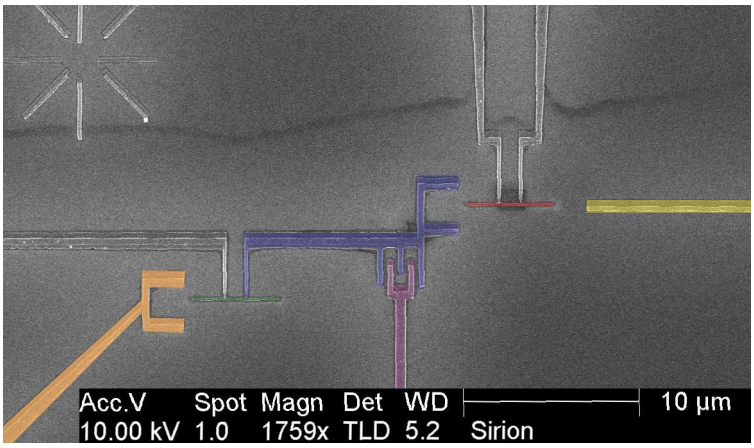

Figure 6.10: SEM micrograph of trap device A with false colors indicating the various circuit elements. The SET island is colored in red and the SET gate is yellow. The trap island is blue, with purple trap gate. The island is green with the gate tinted orange.

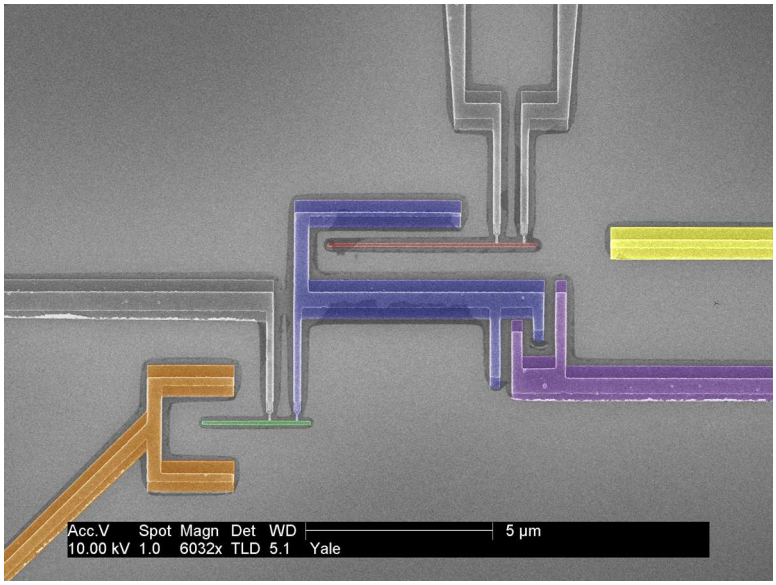

Figure 6.11: SEM micrograph of the final design for trap device B with false colors indicating the various circuit elements. The SET island is colored in red and the SET gate is yellow. The trap island is blue, with purple trap gate. The island is green with the gate tinted orange. The main difference between devices A and B is the higher coupling of the SET to the trap island in device B.

is shown in figure 6.12. The device has shadow islands, designed to be deposited onto the resist

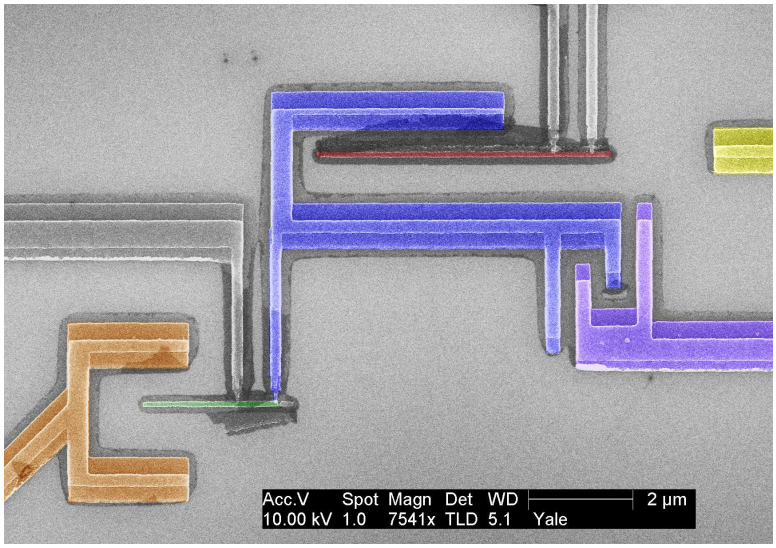

Figure 6.12: SEM micrograph of the actual circuit measured for device B with false colors indicating the various circuit elements. The SET island is colored in red and the SET gate is yellow. The trap island is blue, with purple trap gate. The island is green with the gate tinted orange. The island is shorter than what was intended because it is broken near the end, past the tunnel junctions.

wall that fell back onto the substrate. In addition, the island is broken in a non-critical (but close to being critical) way, which caused it to be shorter than it was designed to be. The experiments worked as planned, but I would not have assumed that the extra metal on the circuit would not have caused problems, and would not have chosen this device if I had seen it before the measurements. Once the fabrication process is complete, the SETs are probed at room temperature with a digital volt meter (DVM) with a 1 MΩ resistor in series.

It takes a few iterations of writing the devices after going through the dose array procedure described in the next section to fine tune the circuit. Once the doses are set, I write as many devices as possible. The devices are extremely sensitive to electrostatic discharge and many are destroyed in the process of mounting them in the fridge. Having many copies increases the chance of successfully cooling down a "live" device. The devices are stored in a dry box in the lab until I am ready to mount them in the fridge, in order to minimize the aging of the junctions, which increases their resistance. Left in air, these junctions can experience aging that increses the resistance by as much as 100% over approximately 2-3 days. Especially for the SET, it is important to minimize any resistance increases.

6.4.4 Finding the Doses

Junction fabrication is the most time consuming and delicate aspect of this process and is integral to the experiment. As I have pointed out in the sections above, I require junctions that are near the performance limit for our microscope. There are many variables in this process, some of which we have more control over than others, for example temperature, humidity, and vibrations in the building. My method for finding the doses for the junctions is an effort to make this a more controlled, scientific process. The total time to go from a circuit diagram to a completed circuit ready for fabrication can be as little as two weeks using this method when the fabrication equipment is functioning normally, but even during that time, the parameters of the process can drift, and we adjust the doses to compensate. While I try to minimize the effects of these parameters that we do not directly have control over (for example, by storing the developer in a temperature regulated water bath), it is crucial to minimize the sensitivity of the fabrication to these variables. The goal of this process is to find an area of parameter space that is maximally insensitive to this drift.

Once the design is finalized, the first step in the fabrication process is to make a massive dose array. I fabricate many copies of the center area of the circuit, without the bond pads and connecting wires, with varying doses. Figure 6.13 shows an example SET circuit. The magenta regions of the

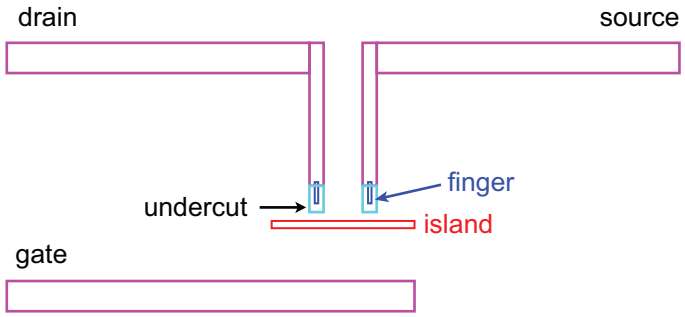

Figure 6.13: An example test device written as one element of a larger dose array. The central part of the circuit including the fingers, island, and undercut are the elements that most directly determine the size of the junctions, and are the elements varied in the dose array. The magenta leads are exposed with a fixed dose such that they can always be fabricated reliably.

circuit have a fixed dose that I have found is high enough so that the features are always well defined. The blue elements are the "fingers," the red elements are the islands, and the cyan elements are undercut boxes. In Figure 6.8 above, you can actually see where the resist boxes have weakened the top layer of the resist, but do not penetrate all the way though. It is these three elements for which

I will do a thorough search of parameter space to find the best doses. The parameter space that is searched for each is the entire range for which there is exposure in the resist. I start with a dose where, for example, the islands won't be exposed and the silicon will be bare and go all the way up to the point where the island is over-exposed and starts to bulge and become wider than the design. The resulting pattern is a 3-D matrix of devices (written one slice at a time on a 2-D chip) shown diagrammatically in Figure 6.14. Each x in the diagram represents a device such as the one shown

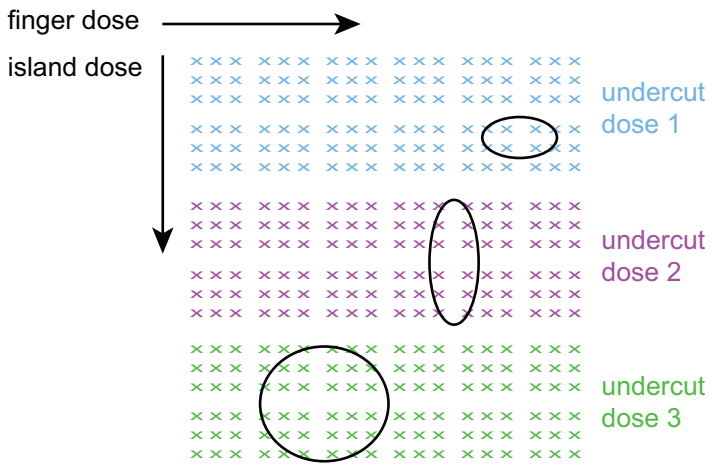

Figure 6.14: Diagram illustrating the dose array that is written to explore all of parameter space for the fabrication of small islands and ultra-small tunnel junctions. The black outlines indicate areas of this space where there are viable tunnel junctions and both the islands and junctions have the intended size and shape. The point of the dose array method for finding the doses is to find the region of parameter space that is least sensitive to drift in any of the fabrication parameters.

in Figure 6.13, and in this case they are written in groups of 9 because that is the area of the field of view of the microscope at the particular magnification chosen for the devices, i.e. the maximum area that can be written without moving the stage. I view nearly all of the devices, spending more time on the areas with viable junctions. The spacing of the doses is a trade-off between precision and time. I will typically write about 400 devices, which in this case took about 2.5 hours to write and more than four hours to view.

The result of this work is that there will be several areas of parameter space that have viable junctions. I have found that it is often the case that the areas have different shapes, and that there is one area in particular that is particularly large and insensitive to dose, as quantified by the sizes of the resulting fingers and islands. These areas of viable parameter space are indicated in Figure 6.14 by the black outlines. It is important to find this stable area of parameter space because there

is always drift from sample to sample, on the time scale of hours to days, in the parameters of the process. If the smallest area of parameter space is found accidentally or through a small scale dose array, it can lead to a longer fabrication effort in trying to follow this drift. The other huge advantage of the dose array method, is that it is not uncommon to misdiagnose under- or overexposure as the opposite effect. All three parameters (finger, island, and undercut dose) are highly related, and you can trick yourself into making wrong choices as you vary the doses if you don't have the additional information that the dose array provides.

Once I find the stable area of parameter space, I write "real" devices, meaning full circuits with bond pads and connecting wires as shown in Figure 6.3. These are much larger (1 mm x 1 mm), and I can typically fit 25 on a chip. Here, I vary the doses over a small range around the center value found in the dose array to fine tune the doses. I will also make a small scale dose array of test devices off to the side for additional diagnostic purposes. I can view the side dose array to get an idea as to what I might have in the real devices without viewing them directly, which is of particular importance for the trap circuit which is cooled blindly. I also have the chance to see what could have gone wrong if there were problems, and have a better idea of how to change the parameters since the small dose array is written under the same conditions as the real devices.

Chapter 7

Experimental Methods and Setup

7.1 Experimental Setup

All of the samples measured in this thesis were cooled in a custom built Cryoconcept dilution refrigerator. The base temperature of this fridge with the magnetic field applied was 18 mK. Early diagnostic measurements for the fabrication process and circuit design were done in a pumped He^3 Heliox system that can reach temperatures around 260 mK. Most measurements were done in the normal state of aluminum, with a magnetic field of 1/2 Tesla applied perpendicular to the aluminum film to suppress the superconductivity. This corresponds to persistent current of 15 A through the superconducting magnet installed in the dewar of the dilution refrigerator. This section will describe the details of the experimental setup.

7.1.1 Sample Holder

The sample is mounted into a "jellyhog"[1] sample holder that was designed to be a standard for all experiments in the Schoelkopf lab. This sample holder consists of a light-tight copper box to shield the sample from RF noise. The chip rests on an interchangeable printed circuit board as shown in Figure 7.1, and a photograph of the jellyhog installed in the fridge is shown later in this chapter in Figure 7.9. The circuit board has standard 50 mil pins soldered perpendicular to the board that bring high frequency signals onto the board. These pins go through the sample holder to SMA connectors and can be connected to the fridge wiring. Traces A-D are these high frequency lines, and the wider strip labeled G is the RF ground for the circuit. Typically there is also a copper trace sitting under the sample in the center of the board, but in this particular case I have removed this

[1] The name comes from the similarity in appearance of this sample to both a hedgehog and a jellyfish due to the tentacle-like cabling sticking out of the top. It can also be referred to as just the "hog" for short.

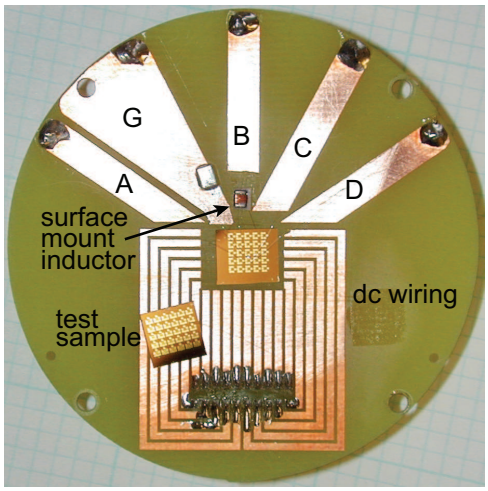

Figure 7.1: Sample mounted on jellyhog board. The chip in the center of the board holds the main device for the experiment. On the circuit board surface, traces A-D connect to high frequency lines through connectors that come out of the under side of the board and are wirebonded to the central chip. Trace G provides an RF ground. Trace B is the RF line as well as the DC bias for the SET, and is wire bonded to a surface-mount inductor and then to the sample. The DC wiring connects to the twisted pair wiring installed in the fridge and is used to bias an additional test circuit on the extra chip.

strip to reduce the capacitance of the bonding pads. I will go into the details of the tank circuit in the next section, where this will prove to be important. The thin lines on the lower part of the board are for supplementary DC measurements. These are low frequency leads that connect to twisted pair wiring installed in the fridge. They go to a connector that is also soldered to the board that goes out to a filter designed in our lab called the tape worm. More details about this filter can be found in Lafe Spietz's thesis [Spietz2006] and in a cond-mat manuscript [Spietz2006a]. This is not important for this work other than the fact that it allowed me to cool down test diagnostic circuits in addition to the main experiment. In Figure 7.1, you can see such a test circuit sitting across these traces. The chips are held down with a thin layer of vacuum grease and the bond pads are wire bonded to traces on the circuit board. Circuit mount components can also be added to the board, and the small inductor mounted just above the chip provides most of the inductance for the tank circuit.

7.1.2 Tank circuit

This section will explain the coupling of RF signals to the SET through a tank circuit, an integral component of the RF setup. This is a resonant LC circuit in which the SET is embedded, as shown in

the diagram in Figure 7.2. The purpose of the tank circuit is to transform the impedance of the SET to match the 50 Ω impedance of the transmission line at a particular frequency with some bandwidth. One can always make a transformer that matches two impedances at a particular frequency, but we will need to optimize the tradeoff between match and bandwidth taking into consideration the band of the amplifier. This section will outline the general formalism for designing the tank circuits used in these experiments. More details on RF design and tank circuits can be found in John Teufel's thesis [Teufel2007].

Figure 7.2 shows a schematic of the tank circuit with respect to the impedance of the lines. For

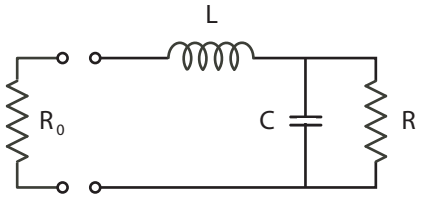

Figure 7.2: Schematic diagram with the tank circuit, consisting of an inductor and capacitor, loaded on the left with the characteristic impedance of the cables R_0 and on the right with a real impedance R.

the purpose of this discussion, I will assume that the lines have a characteristic impedance that is real and equal to R_0, and that the SET has a real characteristic impedance equal to R. The resonant circuit is comprised of an inductance L and a capacitance C. The inductance is mostly from the surface mount inductor shown in Figure 7.1, and the capacitance comes mostly from that of the inductor bond pad and the SET bond pad on the chip. We say that the tank circuit is loaded with this resistance R, and looking in from the transmission line, the input impedance is

$$Z_{in} = \imath\omega L + \frac{R(1 - \imath\omega RC)}{1 + \omega^2 R^2 C^2} \tag{7.1}$$

On resonance, the imaginary part of the impedance goes to zero, so we separate this expression into real and imaginary parts and solve for the resonant frequency

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{1}{R^2 C^2}} \tag{7.2}$$

For most of our devices, R is large enough that

$$\omega_0 \approx \frac{1}{\sqrt{LC}} \tag{7.3}$$

If this is not the case, then R will tend to pull the resonant frequency down. Also, if $R < \sqrt{L/C}$, the imaginary part of the impedance will not go to zero, and there will be no resonance.

On resonance, Z_{in} is purely real and equal to

$$Z_{in}[\omega = \omega_0] = \frac{R}{1 + \omega_0^2 R^2 C^2} = \frac{L}{RC} \tag{7.4}$$

The magnitudes of the imaginary impedances of the inductor and capacitor are equal and we can write down the characteristic impedance of the transformer, which gives us the ratio of the voltage to the current at that particular frequency

$$Z_{LC} = \sqrt{\frac{L}{C}} = \omega_0 L = \frac{1}{\omega_0 C} \tag{7.5}$$

Rewriting Z_{in} in terms of Z_{LC} we have

$$Z_{in}[\omega = \omega_0] = \frac{Z_{LC}^2}{R} \tag{7.6}$$

When this is matched to the impedance of the line

$$R_0 = \frac{Z_{LC}^2}{R} \tag{7.7}$$

$$Z_{LC} = \sqrt{R_0 R} \tag{7.8}$$

In other words, the characteristic impedance of the transformer on match is the geometric mean of the two loads, and ideally we would choose a tank circuit that had this exact characteristic impedance to match our device perfectly to the transmission lines. There are two additional issues to consider however, when designing the tank circuit. The first is the bandwidth of the resonance. There will often be a tradeoff in the experiment between bandwidth and match. We define the bare Q, which is the quality factor the LC circuit loaded by R_0 of the transmission line of this circuit as

$$Q = \frac{Z_{LC}}{R_0} \tag{7.9}$$

which on match

$$\frac{R}{Z_{LC}} = \frac{Z_{LC}}{R_0} \tag{7.10}$$

$$Q^2 = \frac{R}{R_0} \tag{7.11}$$

giving a bandwidth of $B = \omega_0 / 2\pi Q$. The loaded quality factor, which is additionally damped by the resistance of the device is given by

$$Q_L = \left(\frac{R_0}{Z_{LC}} + \frac{Z_{LC}}{R} \right) \tag{7.12}$$

The bandwidth of the tank circuit depends both on the resonant frequency and on square root of the ratio of impedances. Especially as the device resistances become high, a good match is achieved with a sacrifice in bandwidth. The other consideration is that we cannot choose arbitrary values of L and C for the tank circuit. The capacitance does not come from a separate component but is from the SET bond pad as well as any other stray capacitance after the inductor. To minimize this, I have removed the copper trace from the circuit board on which the chips typically sit. I have also mounted the surface mount inductor upside down with it's solder pads sticking up so that I don't add any metal by soldering them down. With these chip inductors that we use, a copper wire is wound to make the inductance and is stuck into the solder pad, and I wire bond directly to the wire itself. The inductor is also mounted up on a teflon brick to keep it further away from the metal traces on the board. The size of the SET bond pads on the chip contributes to the capacitance, but they are made to be just large enough to have 2, possibly 3 bonding attempts and cannot be made smaller. (Bonding to the SET bond pad is not difficult, but bonding to the inductor wire with the inductor up on the teflon brick is very difficult.) As for the value of the inductances, the surface mount components come in discrete values, which also limits the selection for the tank circuit. It would be possible to make a lithographically defined tank circuit, but this was not pursued for this work.

The process of designing the tank circuit to have the best combination of match and bandwidth is to minimize the capacitance and estimate what it is likely to be. Then pick an inductor that will get closest to match. A rough estimate of the tank circuit resonance is made by measuring the reflected power as a function of frequency before bonding up the device. The main effect that bonding the device will have is to pull the resonant frequency down, but this is a useful first step, especially if the resonance frequency is already too low for the band of the amplifier. The tank circuit can really only be tested cold, because the conductance of the silicon will alter the results at room temperature. It is hard to get this exactly right the first time, and this was part of the characterization that was done in the Heliox, which is a smaller system than the dilution refrigerator with a faster turn around time.

The chip inductors we use are from Coilcraft, and for the latest experiment, the particular inductor I used was the 0805-CS-471 with a nominal inductance of 470 nH. The chip inductors aren't perfect lumped elements, and the inductance is frequency dependent. We do not measure the impedance of the tank circuit directly, but measure the reflection coefficient Γ, or S_{11} as measured

with the network analyzer. The reflection coefficient is given by

$$\Gamma(\omega) = \frac{Z(\omega) - Z_0}{Z(\omega) + Z_0} \tag{7.13}$$

where $Z(\omega)$ is the frequency dependent impedance of the tank circuit and Z_0 is the impedance of the line. The reflection coefficient as a function of frequency is shown in Figure 7.3 for two bias points of a SET. Taking the difference between these curves and plotting in linear power units give Γ^2 as a

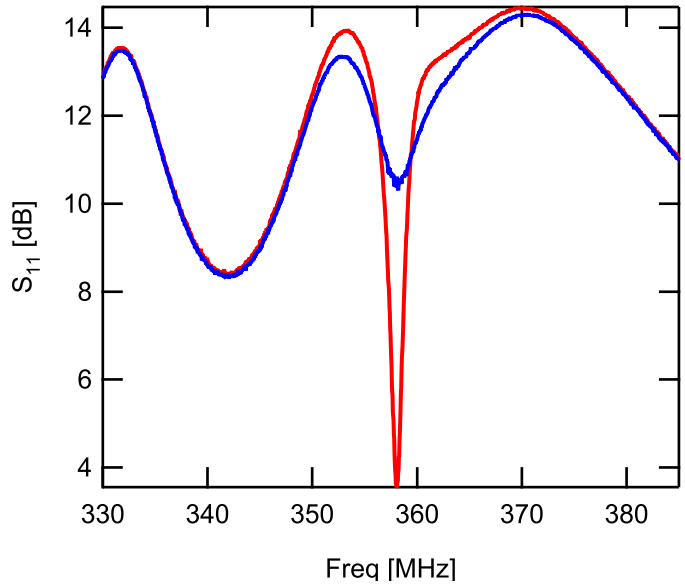

Figure 7.3: Measurement of the reflection coefficient for a tank circuit that matches to an SET with normal state resistance $R_N = 454k\Omega$ at the maximum and minimum match. These two points correspond to different locations in drain-source voltage bias. The extra curvature in these two traces is due to standing waves in the setup which are not calibrated out in the network analyzer measurement.

function of frequency shown in Figure 7.4. The half-width at half max gives the Q of the tank circuit (the full width at half max, FWHM, gives the loaded Q). The total inductance, including that of the wire bonds, ended up being about 660 nH at $\omega_0 = 354\ MHz$. The amplifier I used has a center frequency of 350 MHz. The quality factor Q of the resonance measured cold was approximately 300, giving $Z_{LC} = 1.5\ k\Omega$,which corresponds to a capacitance of 0.3 pF.

7.1.3 Wiring

An important aspect of the setup of this experiment is keeping the sample cold, and this is particularly important to keep in mind when installing transmission lines to bring the signals from room

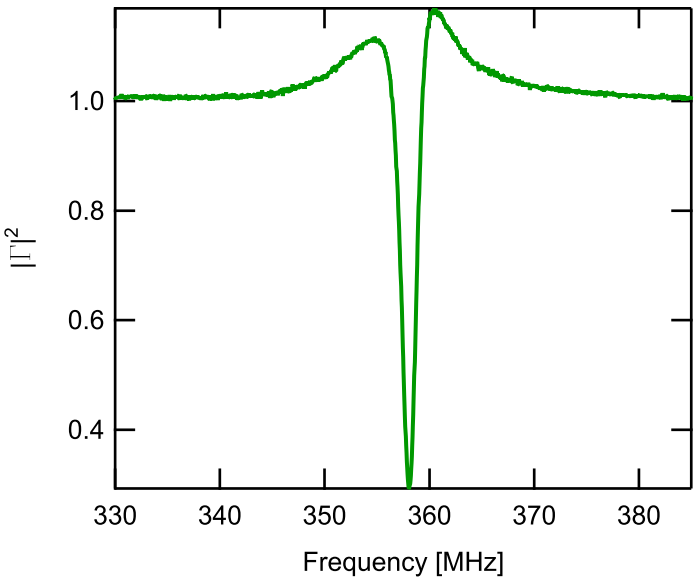

Figure 7.4: Measurement of the reflection coefficient describing the match of the SET to the 50 Ω lines. This measurement is the difference between the two curves shown in figure 7.3, plotted in linear units and squared. The half-width at half-max of this curve is the quality factor of the resonance. Standing waves in the total circuit which includes all of the cabling in the cryostat complicate this measurement. The fact that $|\Gamma|^2$ goes above 1 indicates that the circuit is not exactly described by this simple model, but is not important for the measurements.

temperature to and from the sample. Semi-rigid 0.085" cables bring signals down to the jellyhog in several stages. These particular cables are chosen because they have 50 Ω impedance over a wide range of frequencies and work well with commercially available connectors. They can also be purchased in several different varieties, depending on the thermal and signal requirements. The three types used in this cryostat are UT-085-TP, UT-085-SS, and UT-085-SSSS. UT stands for the original manufacturing company, Uniform Tube Incorporated. The TP cables have silver plated copper weld (SPCW) inner conductors with a tin plated (TP) outer conductor. These are used anywhere there is no thermal gradient, e.g. connecting components at base temperature or for room temperature electronics. These cables have the highest thermal conductivity and are also the cheapest ($\sim \$2/ft$) and easiest to work with. The SSSS cables have stainless steel inner and outer conductors. These cables are the most difficult to work with, are the most expensive ($\sim \$45/ft$), and have the lowest electrical conductivity. They also have the lowest thermal conductivity and are required to make the steep thermal gradient between 4 K and base temperature (18 mK). This distance is approximately 1.5 feet, and the transmission through these cables as a function of frequency is shown in Figure 7.5. A photo of the SSSS cables installed in the fridge is shown in Figure 7.9. The cables are looped

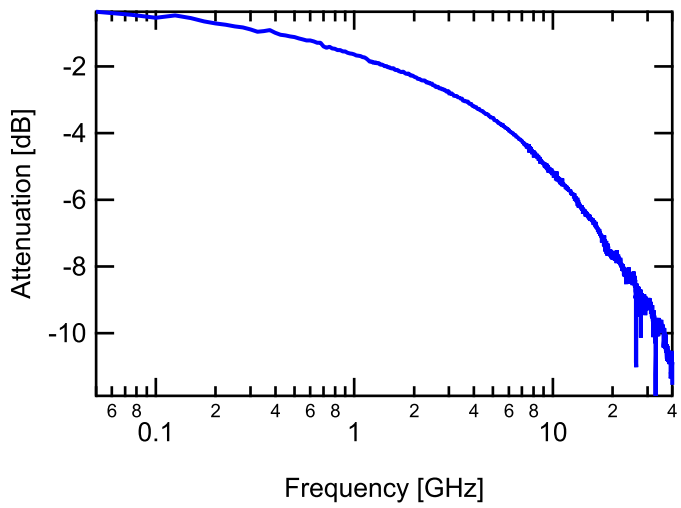

Figure 7.5: Attenuation as a function of frequency of SS-SS semi-rigid cables. This type of cable has the lowest thermal and electrical conductances per unit length and is used to carry signals between 4K and the base temperature of the cryostat. The total length used is approximately 1.5 feet.

at the top into "trumpets" to minimize the stress on the connectors from thermal expansion and contraction of the cables. The cables are clamped at each temperature stage of the cryostat to

thermalize them on the way down to base. The clamps also provide mechanical stability for the connectors. This is helpful because any twisting of the cables tends to either crack the solder joint to the connector, or, depending on the type of connectors used, can cause it to become unscrewed. In the location where the cables connect to the bottom of the 4K plate, the connectors are not visible, so it is important to take extra precautions to prevent cable and connector damage. The SS cables have a SPCW inner conductor with a stainless steel outer conductor. These cables are used to connect from room temperature feed-throughs down to the 4 K plate and are $\sim \$21/ft$. These cables are about 5 feet long and go directly through the helium bath. Since the RF signal has to pass twice through these cables, we do not want to have the high attenuation that the SSSS cables have. These cables are also submerged in liquid helium and are used at higher temperatures, so we can tolerate a slightly higher heat load here. Note that the attenuation as a function of frequency of these cables (figure 7.6) is similar to that of the SSSS cables, but these are almost four times longer.

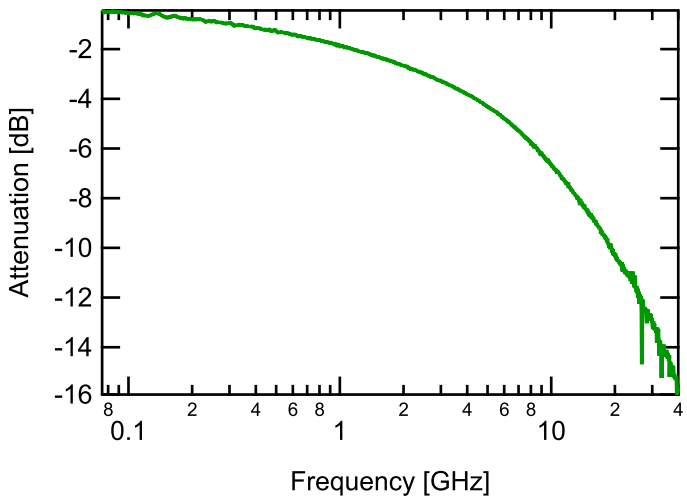

Figure 7.6: Attenuation as a function of frequency of SS semi-rigid cables. These cables have both higher thermal and electrical conductivity than the SS-SS cables shown in Figure 7.5. These cables are used in the helium bath between room temperature and the 4K plate of the cryostat. The total length is approximately 5 feet.

These cables are heat sunk through copper clamps attached at alternating baffles through the bath.

We bring the cables into the fridge from room temperature with a set of feed-through flanges with hermetic glass beads. Similar feed-throughs are used to go through the 4 K plate into the inner vacuum chamber of the cryostat. These beads must be a special type manufactured by Tyco, and are vacuum tight to liquid helium. If the same glass beads that were used at room temperature are used

here, they will typically start to leak after about five thermal cycles. These beads are expensive and difficult to find because the manufacturing company is out of business and they were not designed for cryogenic use, which is why they are not used at the room temperature stage. A photograph of this flange, with and without the SMA connectors is shown in Figure 7.7.

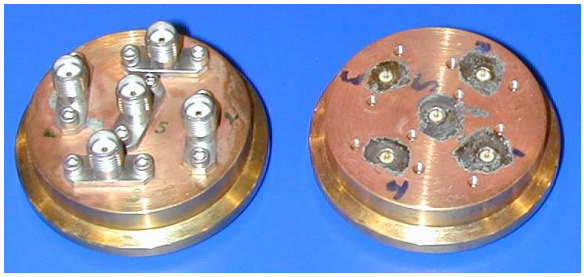

Figure 7.7: Feed-through flanges for the 4K plate. The flange on the right shows the hermetic beads soldered in place, and the flange on the left has the SMA connectors in place. These hermetic beads are a particular type, manufactured by Tyco, that is leak tight to liquid helium.

Two main types of connectors were used for these experiments. This fridge is used by several different people with different experiments. We try to keep as much of the cabling the same to minimize wear and tear on the components. For the cables that stay in the fridge, I have used connectors from Huber + Suhner, part number 11 $PC35-50-2-2/199$. These connectors have a central part that is soldered to the cable and an outer part that screws onto this part. The advantage having two pieces to the connector is that if the cable is torqued, it is more likely that the connector will simply come unscrewed from its base rather than breaking at the solder joint. Over the past couple of years of using these connectors, I have found this to be the case. Another advantage of these connectors is that the gender of the connector can be changed without having to remove the cable or solder any parts together. The downside is that they are approximately three times the price of the AEP sma connectors, part number 9401-1583-010. We use these connectors on the cables that are removed from the fridge when the experiments are switched and for the room temperature cables. The Huber + Suhner connectors also work to higher frequency than those from AEP, but this is not a concern for this experiment.

7.1.4 RF Measurement Chain

A schematic diagram of the RF measurement chain for this experiment is shown in Figure 7.8. Photos of the setup are also shown in Figure 7.9. Radio frequency signals are launched from

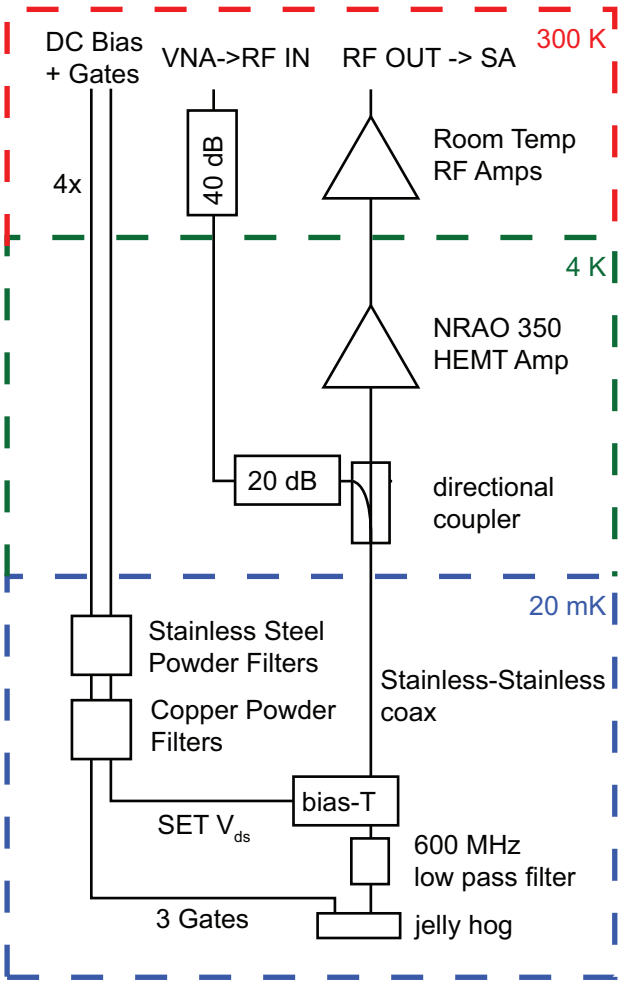

Figure 7.8: Schematic of RF setup used in dilution refrigerator experiments.

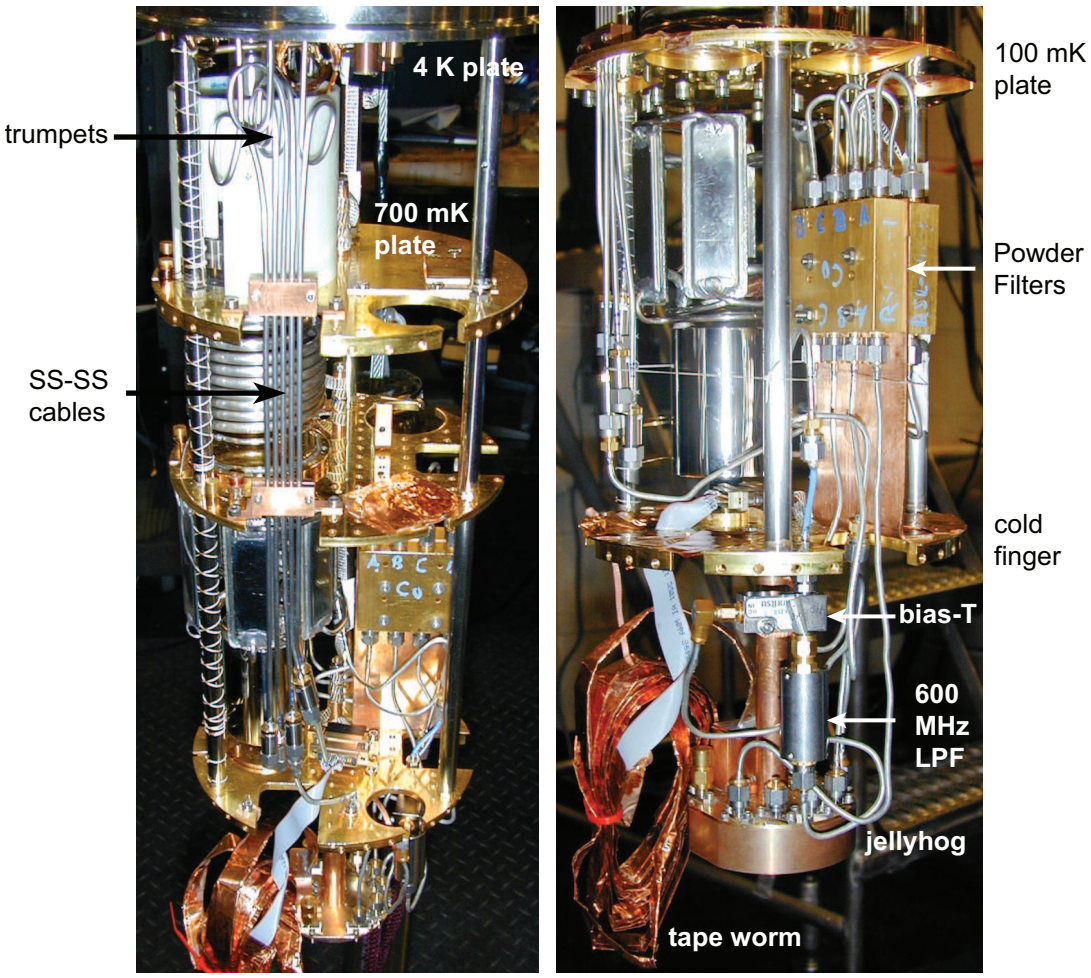

Figure 7.9: Photographs of cryostat with wiring and components inside the inner vacuum chamber. Two angles are provided to have different views of the components. The configurations in the two pictures are also slightly different.

a vector network analyzer (VNA) or RF generator at approximately -20 dBm. The signals are attenuated at room temperature by 40 dB with an additional 20 dB attenuator just before the signal goes into a directional coupler[2]. After the directional coupler, the signals continue down through an Anritsu K250 bias-T, which allows us to add any DC signals from the left port to a high frequency signal from the top port. The signal then goes through a 600 MHz low pass filter to eliminate high frequency photons and down into the jellyhog. The signals are reflected back and travel back through the directional coupler through to the amplification stage.

This experiment has three stages of amplification. The first is a low noise temperature cryogenic high electron mobility transistor (HEMT) amplifier with a center frequency of 350 MHz. This particular amplifier was constructed by Rich Bradley at the National Radio Astronomy Observatory (NRAO). The gain and noise temperature curves for this amplifier are shown in Figure 7.10. As

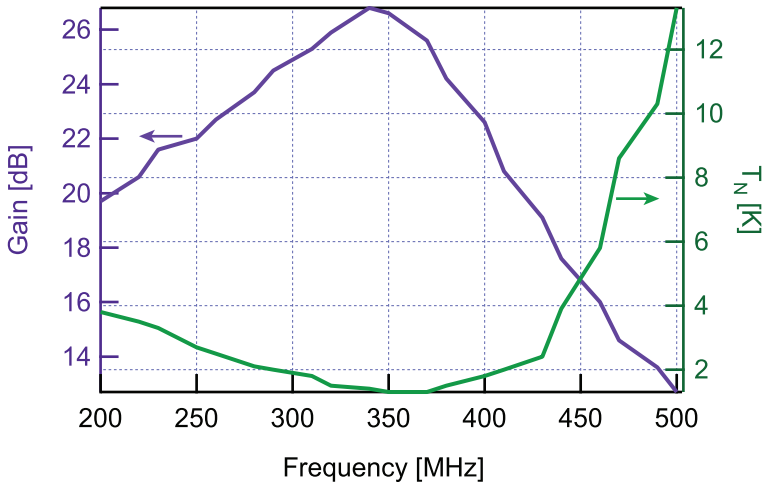

Figure 7.10: Noise temperature and gain as a function of frequency for NRAO 350 MHz room temperature amplifier. This amplifier is located just above the 4K plate submerged in the liquid helium bath and is the first stage of amplification for the experiment. This measurement was supplied by Rich Bradley at NRAO and was taken at 14 K.

shown in Figure 7.8, this amplifier is installed just above the 4 K plate and sits in the helium bath. The next two amplification stages are grouped together in Figure 7.8 as the "Room Temp RF Amps." The first stage of this amplifier group is a relatively low noise temperature ($\sim 20\ K$) 350 MHz NRAO room temperature amplifier whose gain and noise temperature are shown in Figure 7.11. This amplifier is followed by two stages of higher noise temperature Minicircuits LN500 wide

[2]The directional coupler does exactly what its name suggests: the signals going through the port on the left travel down through the lower port. On the way back, signals entering the lower port go straight up through the top port. The particular one used in this experiment is model C4238-10 manufactured by MAC Technology Inc.

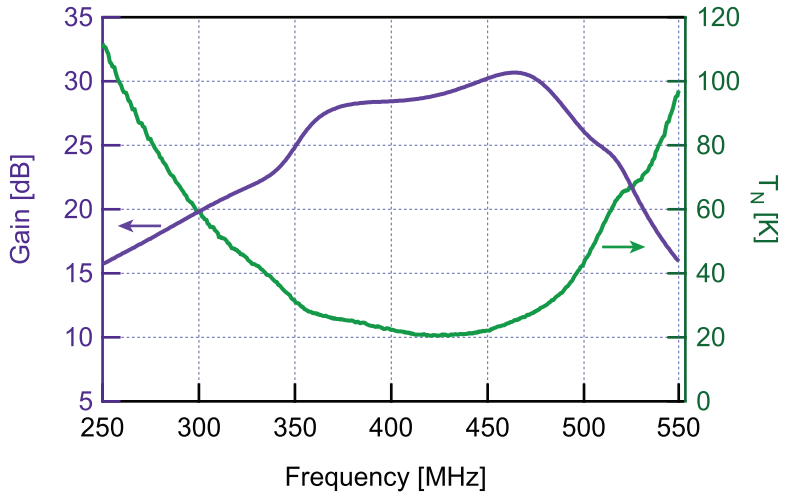

Figure 7.11: Noise temperature and gain are plotted as a function of frequency for the NRAO 350 MHz room temperature amplifier. This is a relatively low noise amplifier that follows the low noise HEMT amplifier shown in figure 7.10. In the measurement, this amplifier is followed by the two Minicircuits LN500's shown in Figure 7.12.

band amplifiers (see Figure 7.12 for gain and noise temperature). Small attenuators (3 dB) are connected between each stage of room temperature amplification to damp any standing waves. The signal is then demodulated using a HP E4407 spectrum analyzer (SA). We take the signals from the video out port with tunable bandwidth that can be set depending on the needs of the experiment. Signals are read into the computer using an 8-bit pci Acqiris Digitzer card, model DP110. More details about the measurement process will be given in the section on RF Measurements.

A parallel set of semi-rigid cables installed in the cryostat carry the gate signals for the experiment as well as the drain-source bias for the SET. These lines connect through the helium bath and go all the way to the cold finger of the fridge. At base temperature they go through two stages of powder filters which consist of about a meter of wire going through a copper block filled with metallic powder suspended in epoxy [MARTINIS1987]. The first set is filled with stainless powder and the next with copper powder. The two stages are somewhat redundant, with the copper stage providing better heat sinking and the stainless having less temperature dependence in its filtering behavior. These are low pass filters with a cutoff frequency around 100 MHz and the frequency dependence of the transmission through these filters is shown in Figure 7.13. In addition to filtering out thermal noise from the higher temperature stages in the fridge, they are excellent heat sinks providing thermalization for the center conductors of the coax lines. The gate lines are then connected directly to the top of the jellyhog, while the SET drain-source lead connects to the left port of the bias-T. The gate signals

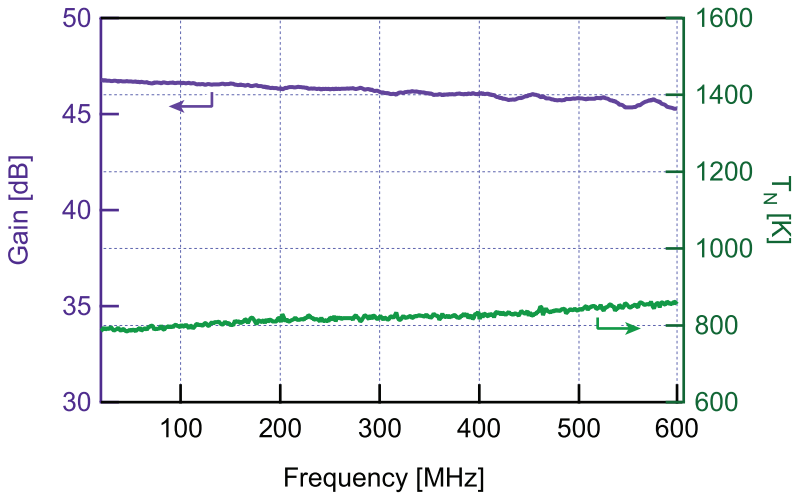

Figure 7.12: Noise temperature and gain are plotted as a function of frequency for the final stage of room temperature amplification. These measurements consist of two Minicircuits LN500 room temperature amplifiers with the two 3dB attenuators that are used in the experiment to damp standing waves between amplifier stages.

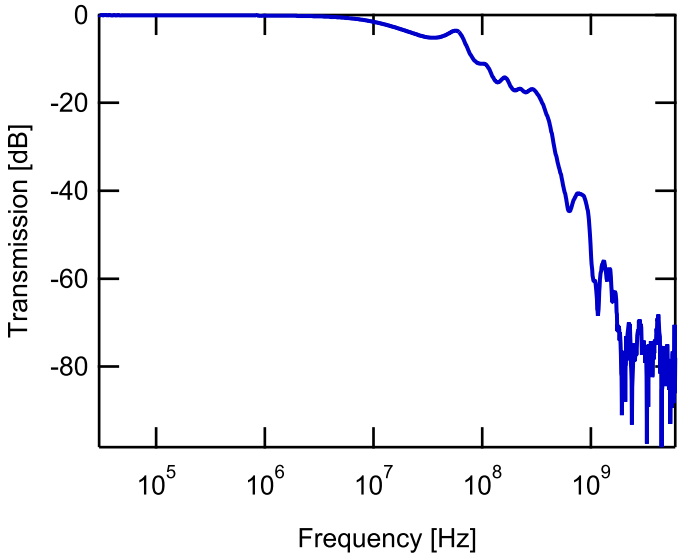

Figure 7.13: Transmission through a copper powder filter as a function of frequency. The copper powder filters serve both as low pass filters to filter out high frequency noise and as thermal heat sinks for the center pins of the transmission lines. These filters are used on all of the gate lines as well as the dc-bias for the SET. These filters are low loss at low frequencies until they cut off steeply above 100 MHz.

are generated by a set of Agilent 33250A arbitrary waveform generators.

7.1.5 DC Measurement Chain

The main DC component of this measurement setup is the drain-source bias for the SET which is biased with a high precision Yokogawa 7651 voltage source. The SET is typically biased through the circuit shown in Figure 7.14 which is enclosed in a metal box at the top of the cryostat. The

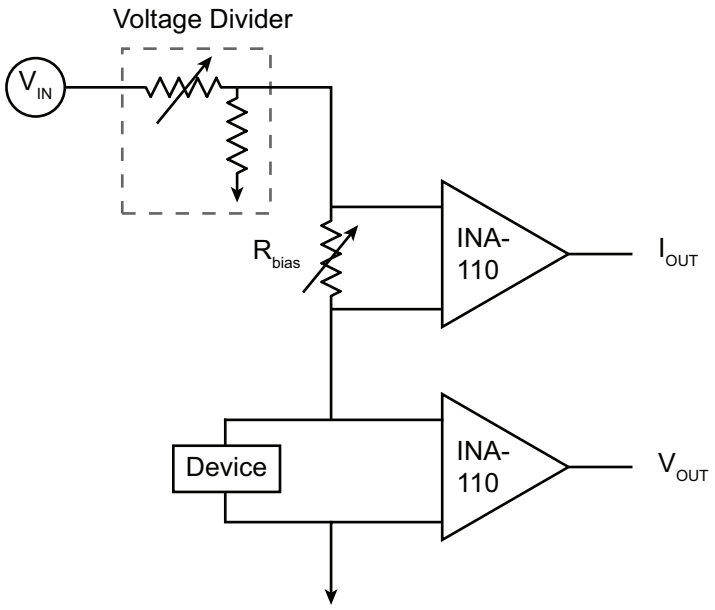

Figure 7.14: Schematic of DC bias electronics for the SET drain-source. A high precision voltage source first divided by a voltage divider with a selectable value, and then applied across the sample through a bias resistor, R_bias. Current measurements are made by measuring the voltage drop across the bias resistor, and voltage measurements are taken at room temperature across the sample. Both the current and voltage taps are amplified by INA-110 instrumentation amplifiers. This circuit is contained in a metal box located at the top of the cryostat.

first stage of this circuit is a voltage divider where the signal from the Yokogawa is typically divided down by a factor of 1000. This minimizes the effects of any noise picked up in the cabling outside the cryostat because the signals can be kept larger than needed up until this point. The other component is a selectable bias resistor for doing DC current measurements and is turned to zero for the high frequency measurements. The bias box also has controls for safely shorting the device. Current measurements are taken by measuring the voltage drop across the bias resistor, and the voltage measurements are a measurement of the voltage drop across the device at room temperature. Both the I_{out} and V_{out} leads are amplified by INA110 instrumentation amplifiers and measurements

are taken with Keithley 2000 digital volt meters (DVMs). The DVMs are connected to a PC running Labview via GPIB.

There is also a set of 20 twisted pair wires (10 pairs) that connect through the jellyhog to the tape worm. The wires come out to a breakout box with BNC connectors and can be used with the same bias electronics that are used to bias the SET. This wiring is useful for characterizing additional test circuits, but is not used in the main experiment.

7.2 RF-SET Operation and Characterization

In this section, I will describe the characterization of the SET in the normal and superconducting state. I will start with brief DC characterization, but the bulk of the measurements are done at high frequency (350 MHz) because of the increased bandwidth and sensitivity. I will show the parameters of the SET and how we find the optimal bias points for doing sensitive charge measurements. I will wait to tabulate the capacitances of the entire device, including the trap, until the next chapter, which goes into more detail about the trap measurements and results.

7.2.1 DC Measurements

Measurements of drain-source current as a function of drain-source voltage are done using the bias electronics described above using a 100 $k\Omega$ bias resistor. Figure 7.15 shows one such measurement done with a slow modulation of the SET gate to show the envelope of current modulation. The normal state resistance of this device is 454 $k\Omega$, measured in the linear region of the IV curve.

7.2.2 RF Measurements

The RF measurements are taken with the spectrum analyzer set to zero span mode at the resonance frequency, in this case 354 MHz. In this mode, the 354 MHz signal is demodulated with a bandwidth set by the resolution bandwidth of the spectrum analyzer. The signal on the screen is the time domain signal, and is output to the computer using the video out port. There is also a video bandwidth that is typically chosen to be equal to the resolution bandwidth.

The first high frequency characterization of the SET is the calibration of the SET gate capacitor. An example of one such measurement is shown in Figure 3.9b. Once this gate is calibrated in terms of applied electrons on the gate capacitor, we measure the Coulomb diamond, which is the reflected power as a function of both drain-source voltage, V_{ds}, and gate voltage, V_g. This is shown for an

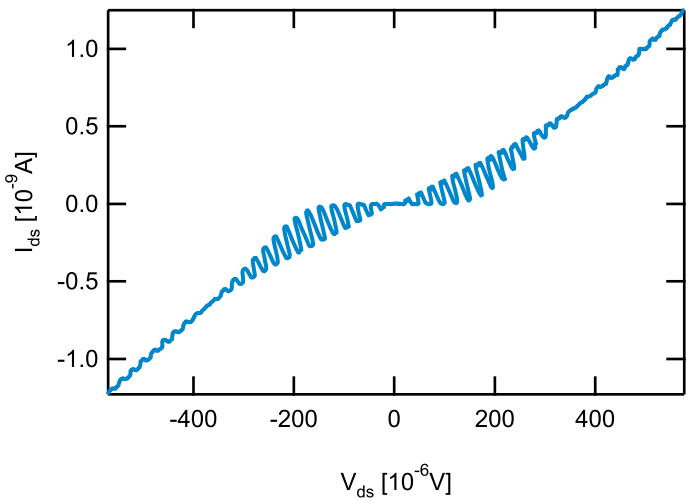

Figure 7.15: SET drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) measured with a slow modulation of the gate voltage by one electron to show the envelope of modulation.

SET in the superconducting state in Figure 7.16 with labels indicating the charging energy and the superconducting gap. The features in the superconducting diamond are sharper than those in the normal state diamond, and there are also additional features that are not present in the normal state, such as the superconducting gap, the lines indicating the Josephson quasiparticle (JQP) cycle, and the peaks of the double Josesphson quasiparticle (DJQP) cycle. These features are not present in the normal state, but provide additional checks on the value of the charging energy. The Coulomb diamond is also shown again in the normal state in Figure 7.17. The rest of the measurements are done in the normal state, so unless it is indicated otherwise, this should be assumed for the rest of the thesis.

Most of the charge measurements done in this thesis are performed at $V_{ds} = 0$. The transfer function of the SET is the measurement of reflected power versus V_g. At low temperature and low carrier power, the Coulomb peaks of the transfer function are very sharp as shown in Figure 7.18. As we apply higher carrier powers, these peaks become broader and smoothed out into a near sinusoidal form out as shown in Figure 7.19. This is a well understood process, and is not heating of the sample. The large ac amplitude from the high applied carrier power samples a wider range of drain-source bias voltage. The fractional variation of the reflection remains unchanged.

The SET is to be used as a sensitive electrometer, so we need to find the carrier power that optimizes the charge sensitivity. This is done by tuning the carrier power while measuring the

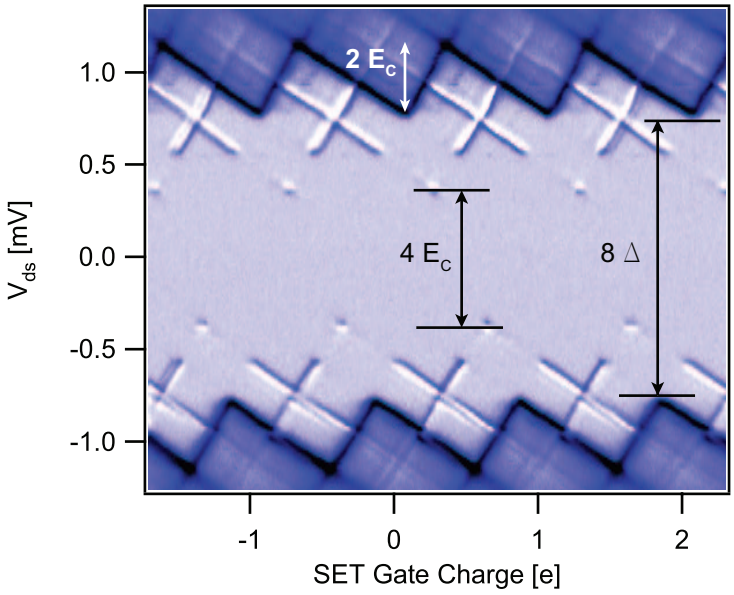

Figure 7.16: A measurement of the Coulomb diamond of the SET in the superconducting state shows the reflected power versus V_{ds} and V_g. The diamond measured in the superconducting state typically has sharper features than the diamond measured in the normal state, and is useful to characterize the SET. There are also additional features not present in the normal state diamond, such as the superconducting gap, the lines from Josephson quasiparticle (JQP) cycle, and the peaks (and valleys) from the double Josephson quasiparticle (DJQP) cycle. The distance between the DJQP peaks is $4E_C$. The total width of the subgap is equal to 8Δ, where Δ is the superconducting gap. This particular SET has $E_C = 2.24\ K$ and $\Delta = 188\mu V$.

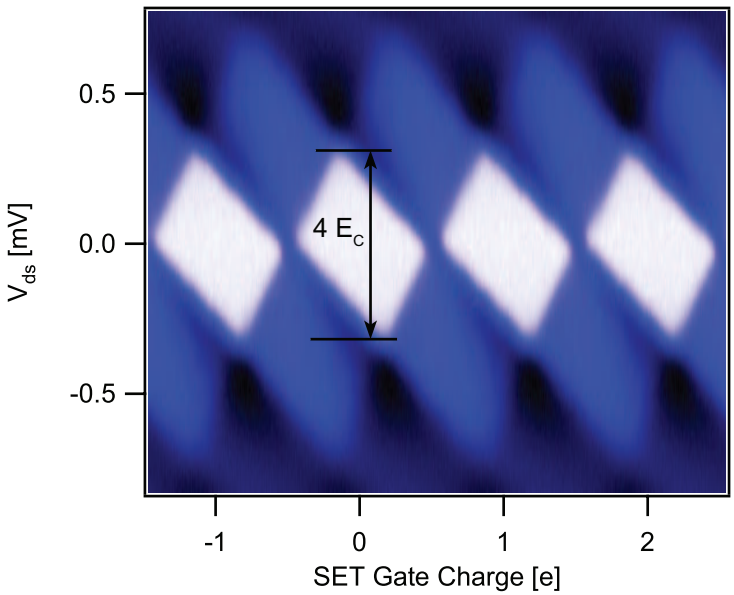

Figure 7.17: A measurement of the Coulomb diamond of the SET in the normal state shows the reflected power versus V_{ds} and V_g measured at the base temperature of a dilution refrigerator (18 mK). The white diamonds in this picture are the regions of Coulomb blockade, and their width is given by $4E_C$. This particular SET has $E_C = 2.24\ K$.

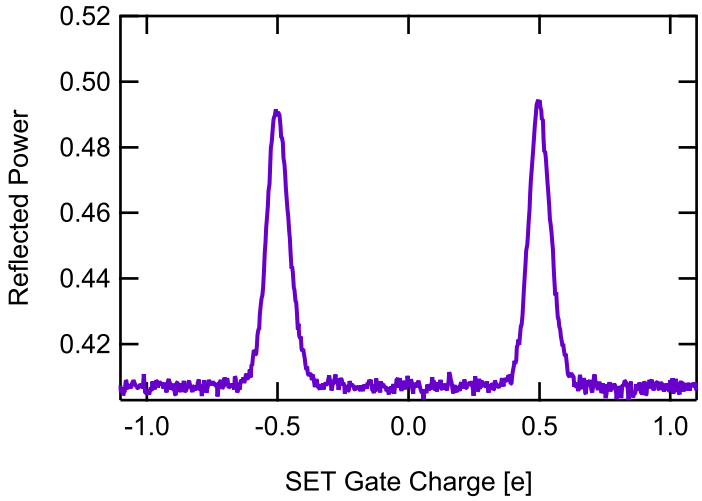

Figure 7.18: Reflected power measurements as a function of SET gate voltage trace out sharp Coulomb peaks. This is a cut from figure 7.17 taken at $V_{ds} = 0$ and a carrier power of -45 dBm, not including the attenuation of the signal into and through the cryostat.

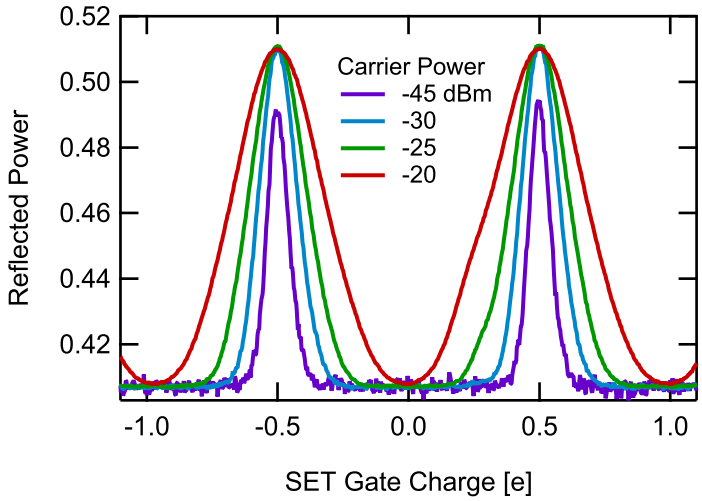

Figure 7.19: Increasing the carrier power broadens the Coulomb peaks. At high carrier power the signal is smoothed out into a near-sinusoidal form because the high ac carrier power samples a wider range of the transfer function. Note that increasing the carrier power from -30 dBm to -20 dBm does not change the fractional variation of the reflection.

charge spectral density of the SET. We measure the charge spectral density by measuring the voltage spectrum of the SET biased at a point that is sensitive to small changes in gate voltage. The voltage spectral density is converted to the charge spectral density by means of a small oscillatory test signal superimposed on the SET gate at a chosen frequency. Since we have calibrated the gate in terms of the number of electrons applied to the SET island, we know exactly how large this signal is in terms of charge. A charge noise measurement for the SET is shown in Figure 7.20. This graph shows the characteristic low frequency charge noise of these devices known as $1/f$ noise due to the motion of charge impurities in the substrate near the device or in the junction barriers. The optimal carrier power gives the highest signal to noise measurements of charge coupled to the SET, so this is the power setting that we will use for most measurements of the trap shown in the next chapter.

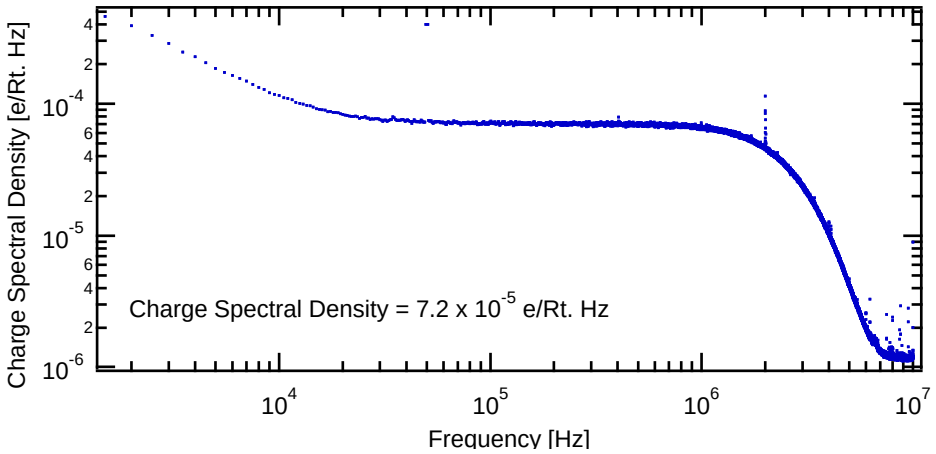

Figure 7.20: Charge spectral density of the SET. The charge spectral density at 1 Hz is $8 \times 10^{-4}\ e/\sqrt{Hz}$

Chapter 8

Time Resolved Single Electron Dynamics

This chapter presents the measurements of the single electron trap. The primary results were achieved with two different samples which I will call A and B. Sample A was measured in the winter of 2006, and sample B was measured in the summer/fall of 2006. Earlier experiments led the way to these results, but will not be presented here. I achieved the first good measurements of the dynamics of the trap with sample A, but was unable to time resolve the tunneling dynamics because the SET from sample A did not have high enough charge sensitivity, and the coupling to the trap was too small. The second sample had an SET with better charge sensitivity and higher coupling to the trap, giving the signal to noise ratio required for measurements in the time domain. The key parameters for these two samples is shown in Table 8.1.

Description	Symbol	Device A	Device B
SET Charging Energy	$E_{C,SET}$	2.24 K	1.66 K
SET Normal State Resistance	R_N	530 $k\Omega$	453 $k\Omega$
Coupling Strength	κ	2.3%	10%
Charge Noise	S_Q	$(2 \times 10^{-4})^2 e^2/Hz$	$(7 \times 10^{-5})^2 e^2/Hz$

Table 8.1: Parameters for devices A and B. The feasibility of the experiments were the combination of the coupling strength to the trap and the charge sensitivity which determine the signal to noise ratio. Both the SET charging energy and the normal state resistance contribute to the charge sensitivity.

This chapter will go through the measurements of the statics of trap experiments and then continue on to look at the dynamics. Both data and comparisons with theory will be presented.

8.1 Statics of the Single Electron Trap

The first step in the trap experiments is careful characterization of the circuits. The circuit diagram is shown again in Figure 8.1. The distinguishing measurement of a single electron trap is the

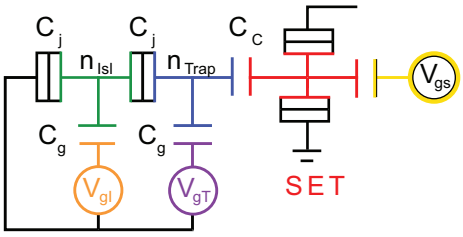

Figure 8.1: Circuit diagram showing the single electron trap measured by the SET.

hexagonal stability diagram introduced in Chapter 2. The technique for measuring the hexagons is analogous to the one I outlined in Chapter 3 in the SET-box example but now I have the added complication of the additional gate. The SET and the trap are biased in the same way that the SET and box were biased in Chapter 3. For fixed island gate, small changes in the trap gate only change the island potential a small amount. The capacitance between the trap gate and the island was intentionally designed to be as small as possible so that I would not have to also countersweep the island gate while sweeping the trap gate. The measurement procedure is to sweep the trap gate, counter-sweeping the SET gate to offset changes in bias to the SET island caused by the trap gate. We record the response of the SET during each sweep. The island gate is then stepped, and the trap and SET gate are offset manually to compensate. I incorporated software that was developed over the last 8 years for the experiments on SET measurements of the single electron box by Konrad Lehnert, Ben Turek, and Johannes Majer to bias the SET and trap gates. It would have been possible to incorporate the third gate into this software, but this was not required to operate the experiment successfully and not worth the added complexity in the software.

Just as in the staircase measurements of Chapter 3, the measured quantity is the sawtooth from which the charge on the measured island is inferred. Figure 8.2a shows the sawtooth measurement for the trap for many values of the island gate charge. I will show more details about these slices and how they are used to characterize the trap, but for now I would like to focus on the hexagon as a whole, as it provides a map of the device parameter space. Figure 8.2b shows the inferred charge on the trap, with labels indicating the charge states of both islands. The sawtooth picture is presented because it provides a higher contrast picture for looking at the hexagon. Focusing on

this first graph (figure8.2a), notice that there is additional noise in cuts of island gate charge near $n_{gIsl} = 0$ that decreases in the direction of $n_{gIsl} = 1/2$. This is not an artifact of the measurement, but offers a hint at the dynamics that underlie this measurement. As I stated in Chapter 2 and discussed in more detail in Chapters 4 and 5, the tunneling rates on and off of the trap island are slowest when the island is in the most blockaded state, at $n_{gIsl} = 0$. The rates are also slowest at the charge degeneracy point of the trap ($n_{gTrap} = 1/2$). This is exactly where the extra noise shows up in the hexagon plot. These measurements are performed sweeping the trap gate as slowly as possible, in this case 100 ms. Between states $(0, 0)$ and $(0, 1)$, for example, there is the energetically forbidden intermediate state $(1, 0)$. This means that on the time scale of the sweep rate, the trap is not always found in the ground state. As the tunneling rates increase with respect to the sweep rate (a constant in this graph), the noise decreases and the charge on the trap is able to follow the charge applied by the gate.

Another measurement taken over many periods of the hexagonal structure is shown in Figure 8.3. This diagram also illustrates the fact that the capacitance between the trap gate and the island

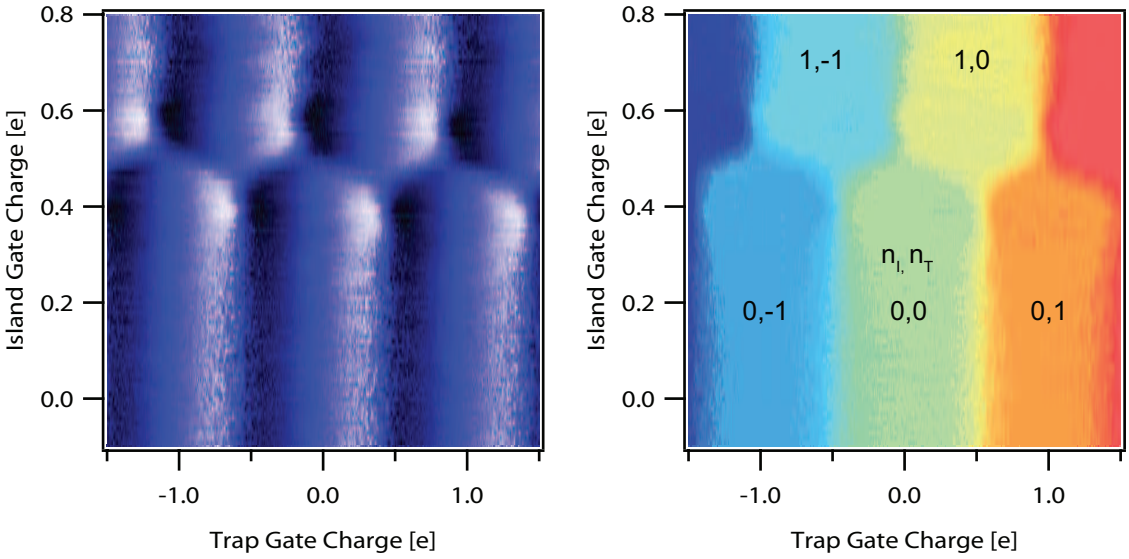

Figure 8.2: a) The hexagon stability diagram of the trap as measured directly. Shown is the SET response as a function of island and trap gates. b) The inferred charge on the trap as a function of both gate voltages. The sawtooth Figure is shown because of the higher contrast that picture provides.

is quite small. If it were not, we would see a tilt in the hexagon pattern, tilting in the direction of positive island gate charge with increased trap gate charge. These hexagons were taken using device

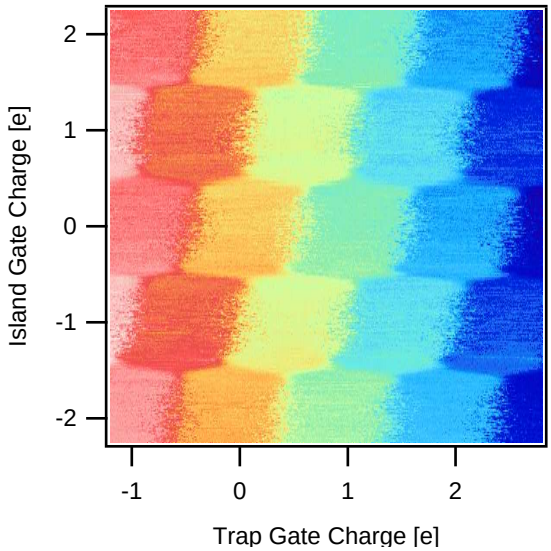

Figure 8.3: The stability diagram of the single electron trap measured with less averaging over many periods. Near the areas of integer charge on the island gate, the rates are very slow (kHz) on the trap island, and the trap island charge cannot keep up with the applied gate charges.

B. In device A, the trap gate was more strongly coupled to the island, and this tilt is more apparent as shown in Figure 8.4.

The hexagon measurements provide a map of the parameter space of the trap and are performed prior to any measurement. There is charge offset noise in all of these devices, so all of the gate biases are relative and can change. The main source of change is the SET, which I will show in more detail in the dynamics section of this chapter. If the charge on the SET changes, then the gate bias must be changed to keep the SET biased at a sensitive operating point. Changing this gate, however, affects all of the islands and changes the location in the hexagon diagram. There is enough stability to take measurements over several tens of minutes, but these conditions will change over the course of the day. A quick hexagon measurement is used between measurements of other quantities to ensure that the trap has not shifted and to correct for any changes that have occurred.

Slices of the hexagon pattern in island gate give the familiar Coulomb staircase of the trap island. One such measurement, performed at 18 mK, is shown in Figure 8.5 with a fit to a weighted Boltzmann distribution (see Chapter 2 for more details). The coupling between the trap and the SET island for this measurement is 10.3%. The rounding of the Coulomb staircase depends on temperature, as expected, but also shows a dependence on the bias point with respect to trap island.

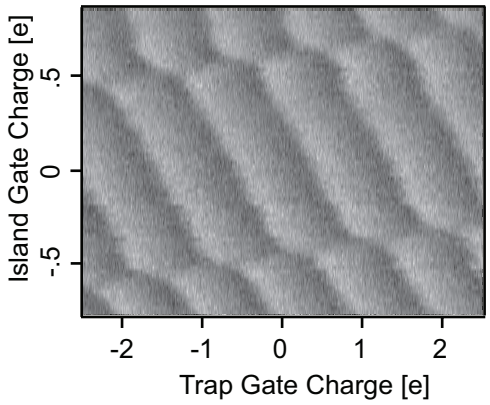

Figure 8.4: The stability diagram of the single electron trap in device A. The cross capacitance between the trap gate and the island is larger in this sample and this causes a slight tilt in the hexagonal pattern.

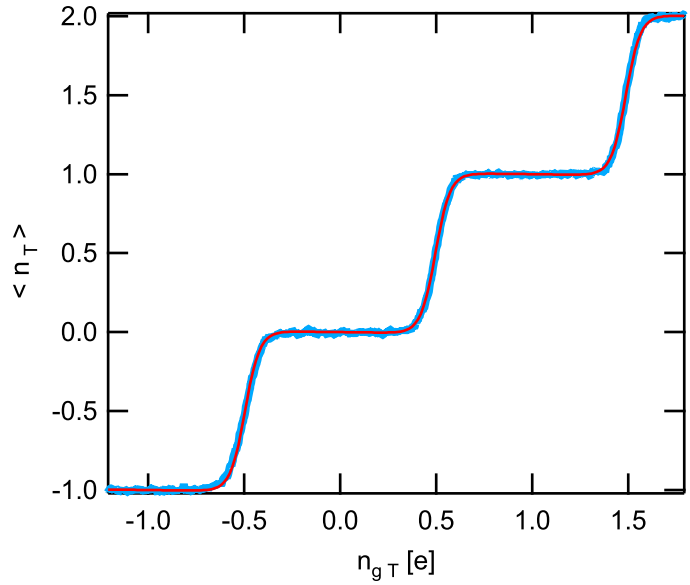

Figure 8.5: Coulomb staircase at of the single electron trap. The average charge on the trap island is measured as a function trap gate,n_{gT} at 18 mK. Shown in red is a fit to a weighted Boltzmann distribution.

This is due to the fact that the trap must be measured much more slowly at the high blockade state because the tunneling rates are so slow at that point. The noise is higher here because the trap does not always settle into the ground state (i.e. we can never sweep slowly enough) and because the measurements take longer and the trap is more susceptible to charge noise over longer periods of time. Figure 8.6a shows staircase measurements for three temperatures, and Figure 8.6b shows measurements taken at 18 mK for the high and low blockade states of the island.

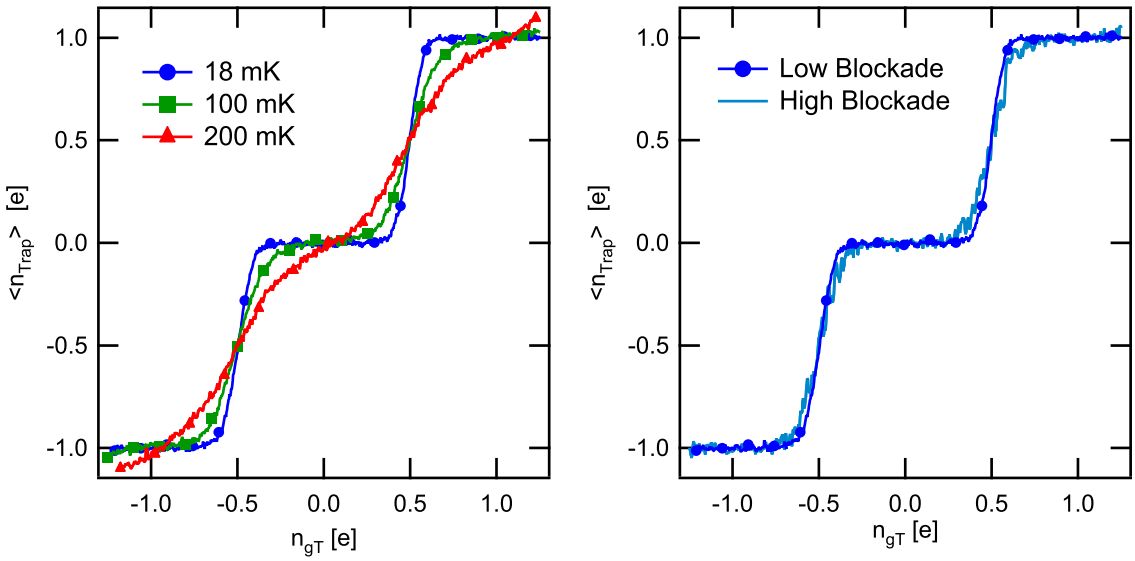

Figure 8.6: a. Coulomb staircase of the trap. The average charge on the trap island as a function of trap gate, measured at 18 mK, 100 mK, and 200 mK with low blockade on the island gate. These measurements, taken at many temperatures, are fit to a weighted Boltzmann distribution (shown in Figure 8.5), and used to extract the charging energy of the trap (see Figure 8.7. b. Coulomb staircase of the trap at 18 mK measured at high blockade of the island gate (middle of hexagon) and low blockade (edge of hexagon).

I have measured the staircase at many temperatures, and use the Boltzmann fits to extract the parameter $\chi = E_C/2k_BT$. When this is inverted and plotted against the fridge temperature, we see the linear temperature dependence and can extract the trap charging energy as shown in Figure 8.7 for the low blockade state of the island. The experiment is well filtered, and the saturation of $1/\chi$ is not thought to be heating. In our group we have been able to measure temperature quantities such as the temperature dependence of the shape of the single electron box [Lehnert2003] and the electron temperature in a shot noise thermometer [Spietz2006] down to temperatures well below this saturation point. This observed rounding comes from two places. The first is that the measurements

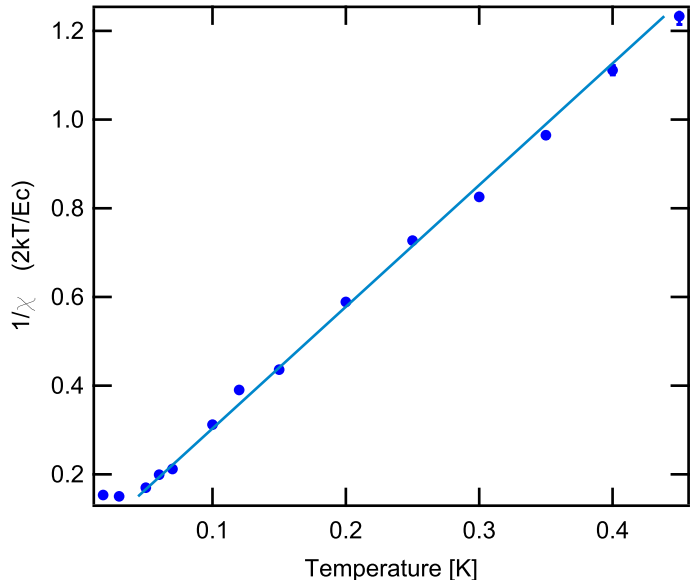

Figure 8.7: The staircase measurements are fit to a weighted Boltzmann distribution as shown in Figure 8.5, and the parameter $1/\chi$ is extracted and plotted as a function of the fridge temperature. A linear fit gives a value for E_C of the trap of $0.727 \pm .007$ K. The error bars for most points on this graph are smaller than the plotted point size.

are taken slowly, and any charge noise in the trap will cause the position of the charge degeneracy point to shift slightly, rounding the staircase. The second place additional rounding comes in is from the backaction caused by the SET. For this device, the forward coupling of the trap island to the SET island is 10%. The reverse coupling, or the percentage of each SET electron that couples to the trap island is higher at 20%. In Figure 8.8, I show the extracted value of $1/\chi$ as a function of temperature for staircases measured both at the low island blockade (shown above) and the high island blockade shown in Figure 8.6b. These additional measurements are even more rounded than the sharp staircases measured for at low island blockade for the reasons described above in the discussion of the staircase measurements. In order to compare the effects of the sweep to that of integrating in additional charge noise, I have measured the high island blockade staircases in a "DC" way. These points are taken by acquiring long (1 s per point in trap gate) time traces of raw data (see the section on time resolved tunneling events in this chapter), and extracting the average charge on the trap directly. Because these traces are acquired so slowly, they are prone to having additional noise integrated in, but they do not suffer from effects caused by sweeping the trap gate too quickly. These points are in agreement with the swept trap gate. Unfortunately, I only have one

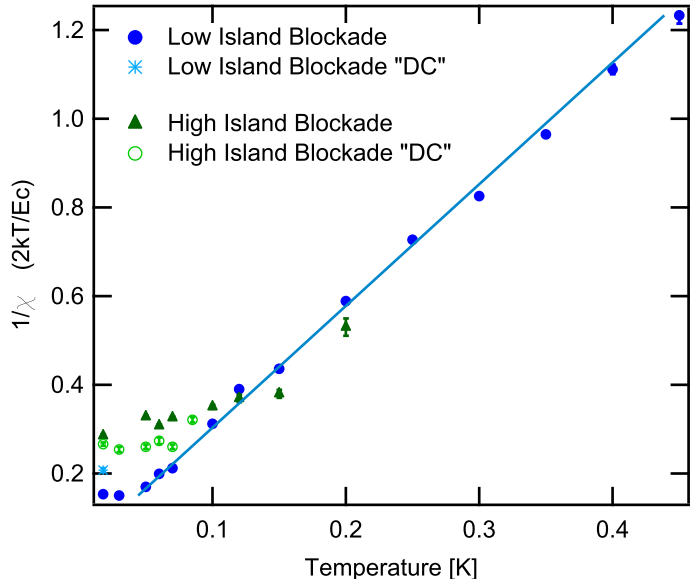

Figure 8.8: This graph shows the linear fit of $1/\chi$ vs fridge temperature plotted in Figure 8.7 as well as the additional staircase measurements at higher island blockade. The fastest tunneling rate occur in the region with low island blockade. In the regions of high island blockade, the rates are so low that it is difficult to sweep the trap gate slowly enough. These measurements take longer than in the region of fast rates because of the low required sweep rate, and any charge motion nearby will cause rounding of the staircase. The data points labelled "DC" were measured without sweeping the trap gate and are taken by acquiring a time trace 1 second long from which the trap charge is inferred.

point acquired using the "DC" method at low island blockade to use to compare the fast rate data to the slow rate data.

8.2 Dynamics of the Single Electron Trap

This section of the thesis will explore the dynamics of the single electron trap that have been measured using several different methods. The first section discusses measurements taken of the charge relaxation time of the trap. I was able to measure the dynamics of the device using averaging techniques to extract the underlying rates. The second section details the time resolved single tunneling measurements, which are the core results of this thesis.

8.2.1 Charge Relaxation Time of a Single Electron

The hexagons have already shown us hints at the dynamics in the trap circuit, as we are never able to really sweep slow enough to keep the trap in the ground state. If we intentionally sweep the trap gate much faster than the characteristic tunneling time and measure the Coulomb staircase, we would expect to see a hysteresis. This is shown for two different settings of the island gate in Figure 8.9. The top axis of the staircase plot is the sweep time, which is the same for both traces. The red staircase (top), is taken at the high blockade point and is very hysteretic because there is a time delay for the trap to relax into the ground state. The blue (lower) staircase is taken at a low blockade point where the rates are much higher and we do not see the same hysteretic behavior. This is a good indication that this is a device that truly has tunable tunneling rates that are adjusted by the bias of the two gates.

To obtain a more quantitative measurement of the tunneling rates as a function of the trap gate, I performed a series of pulsed gate measurements. I first find the highest blockaded island state by performing a measurement of the hexagon, as outlined above. Once the island bias is set, a trap bias is chosen, as indicated by the tick mark at "t=0" in Figure 8.10a. I wait for a time that is long enough to find the trap in its ground state with a high probability. Then, a fast step function is applied to the trap gate, and I measure the charge as a function of time. I repeat this measurement thousands of times, and the end result is shown in Figure 8.10b. For short times, the charge of the trap remains unchanged from the original ground state. Over time, on average, the charge relaxes into the new ground state with some time constant τ. The instantaneous charge on the trap island is still quantized and is equal to 0 or 1. We can think of this as a measurement of the relaxation

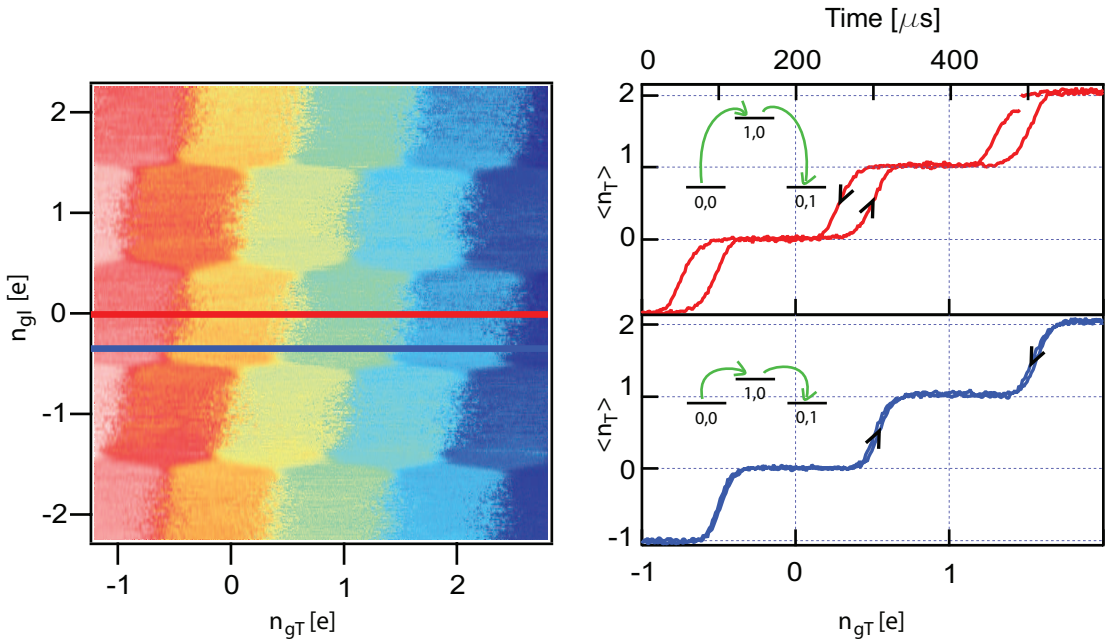

Figure 8.9: At the highest blockaded state of the trap ($n_{gI} = 0$), sweeping the trap gate faster than the characteristic tunneling rate results in a staircase measurement that is hysteretic, shown in the top staircase measurement in red. If the island is not biased at this blockaded state, but at another point where the blockade is lower (blue line), then the tunneling rates are faster, resulting in a staircase measurement swept at the same rate, that does not show hysteresis.

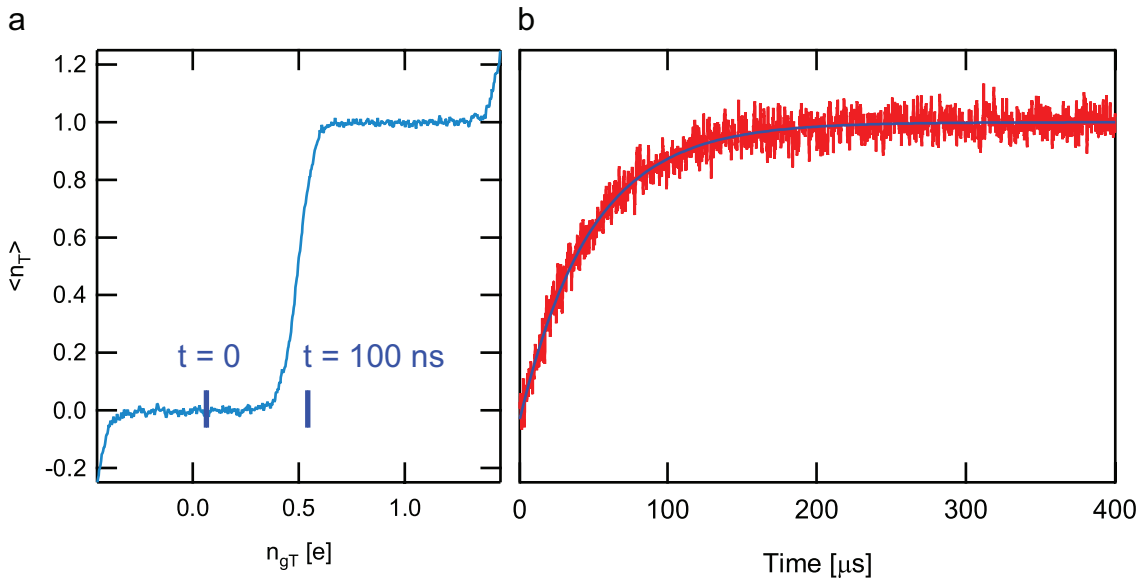

Figure 8.10: Measurements of the charge relaxation time of the trap. a) The measurement starts with a gate bias at some position at t=0, as indicated by the tick mark on the graph. A fast pulse is applied to the gate, shifting it over to the next tick mark within 100 ns. b) The charge of the trap is recorded for 1 ms. The experiment is repeated thousands of times and the resulting measurement of the charge relaxation time of a single electron on to the single electron trap in this case is equal to 47 μs.

time of a single electron onto (or off of) the trap island. We can show that this is not just an RC time in the system both by changing the bias conditions and seeing that these rates change, but also by just applying a fast pulse to the SET gate and observing a much faster response, as shown in Figure 8.11.

This technique is a way to extract the tunneling rates when there is not the signal to noise ratio to time resolve tunneling events, as was the case for device A. This experiment is repeated for many values of trap gate bias and the tunneling rates are plotted as a function of the trap gate bias in Figure 8.12. Also shown in this graph is a theoretical prediction for the tunneling rates in this device. This theoretical model has no adjustable parameters and shows quite good agreement with the data.

8.2.2 Time Resolved Tunnelling Events

This section is the main result of this thesis which is time resolved measurements of single tunneling events in the single electron trap. These measurements were all completed using device B. Because of combined effects of the higher coupling between the trap and the SET and the increased sensitivity

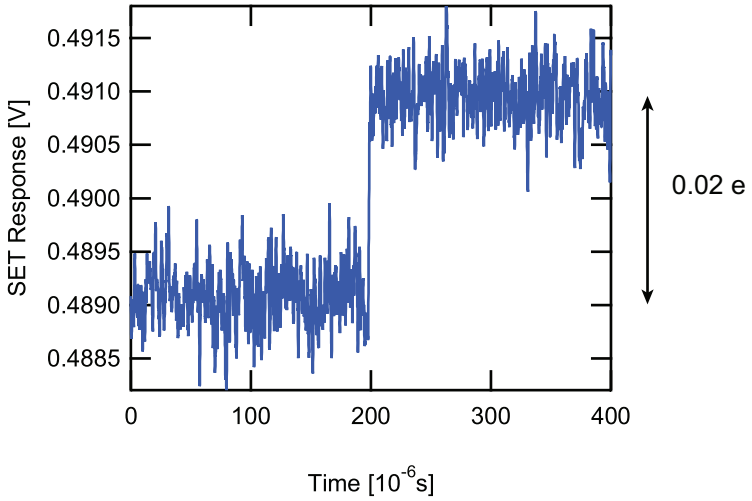

Figure 8.11: This graph shows the fast response time of the SET to a 0.02e gate applied at 200 μs. This response is much faster than the relaxation time of the trap shown in Figure 8.10b.

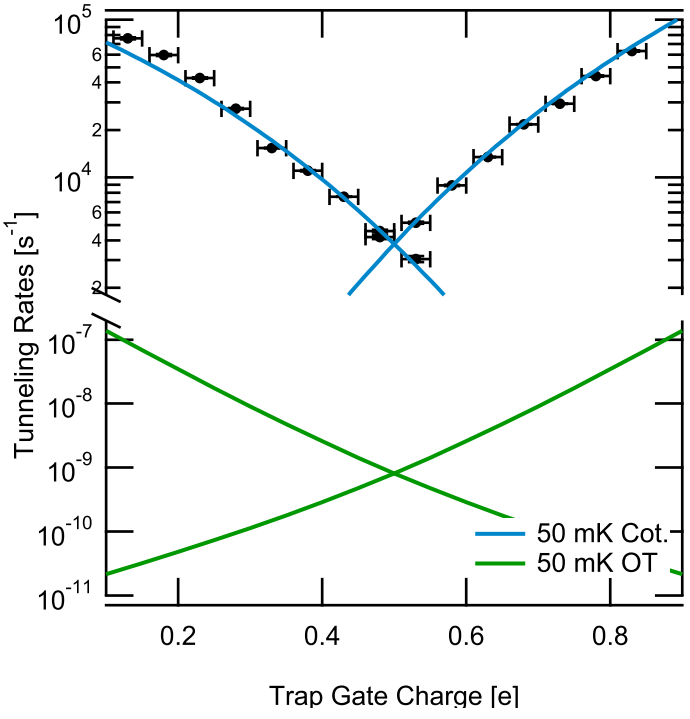

Figure 8.12: Tunneling rates for the trap as a function of trap gate acquired using the relaxation time measurements. The blue theory curve is the 0-parameter cotunneling prediction. The green curve indicates the 50 mK Orthodox theory prediction.

of the SET, I had the sensitivity with this device required to time resolve single tunneling events. In this regime, we can explore measurements that are not possible when averages are required. For example, in all of the measurements of the Coulomb staircase, the quantity measured is always the average charge. If we were able to time resolve the charge on the trap island, we would be able to measure the charge on trap as a function of trap gate, as shown in Figure 8.13. There is still noise in

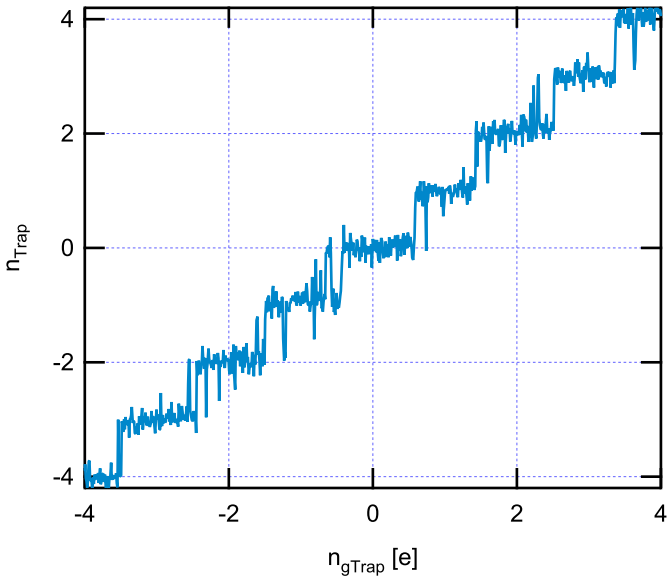

Figure 8.13: A single shot measurement of the Coulomb staircase for the trap. The charge on the trap is quantized in discrete states n. For this data, the trap is swept over 8 electrons in 50 ms.

the measurement, but the quantized nature of the trap charge starts to be visible. On average, the trap charge state changes at the charge degeneracy point, but tunneling is a stochastic process that occurs at a certain rate. Thus, there is always a finite probability to tunnel either before or after the degeneracy point, yielding on average, a smooth transition between charge states. The rest of this chapter will focus on measurements of time resolved single tunneling events and extracting the intrinsic rates for electrons tunneling on and off of the trap island.

The measurement process starts with acquisition of the time domain data as shown in Figures 8.14a,c for two different bias points of the trap gate. The amplitude histograms for these two traces are shown in Figures 8.14b,d. In order to extract the intrinsic rates for electrons tunneling on and off of the trap island, we must work to discriminate between these two states in this noisy telegraph signal. The most obvious thing to do, and what you would actually do if you only had

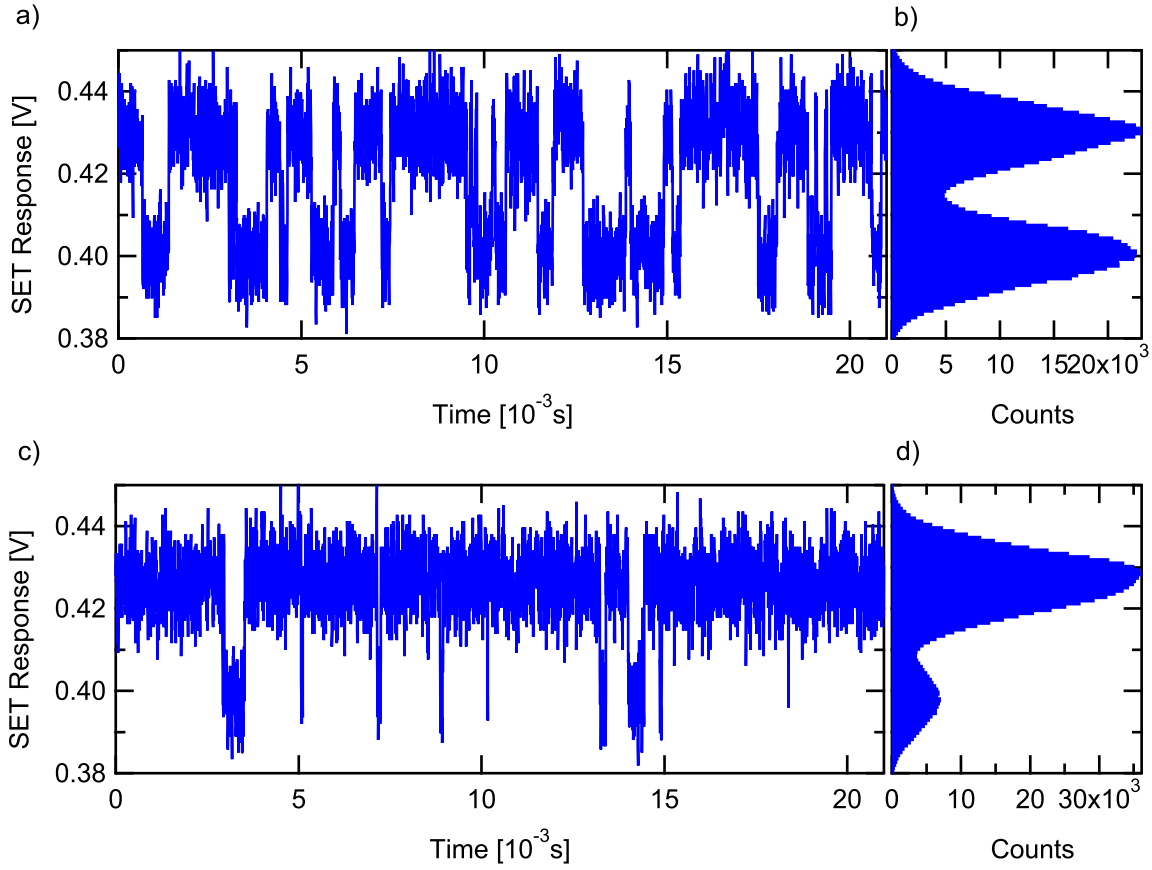

Figure 8.14: Raw time domain measurement of the charge on the trap. Figures a and c show a small segment of the total time trace that is half a second long. Figures b and d show the histograms for the entire time traces. The top graphs are positioned at the charge degeneracy point of the trap, where the tunneling rates are equal and the trap spends an equal amount of time in each charge state. The lower Figures show measurements for a gate bias away from trap charge degeneracy. Here, the trap spends much more time in the 1 state than in the 0 state.

one data point and wanted to make a single shot measurement, would be to set a threshold at the middle of the histogram between the two peaks. Then, everything below that threshold would be counted in the 0 state, and everything above would be counted in the 1 state. You could digitize the data into a stream of 1's and 0's and extract the lifetimes. If the signal to noise ratio is high enough so that there are two distinct, non-overlapping peaks in the amplitude histogram, this is the way to go. If there is any overlap, a statistical approach must be used to separate the events in the overlapping region, which amounts to setting a double, latching threshold for the discrimination. The technique used to analyze the data in this thesis is called a Schmidt trigger, and the procedure that I have used is detailed in Yuzhelevski et al. [Yuzhelevski2000]. The assumptions of this model are that the single electron tunneling events are Markov processes and that the noise in each state is Gaussian. This model would give two delta functions in amplitude broadened by Gaussian noise, which is exactly what I have observed. This procedure aims to assign each point in the time trace to one of the two states, creating a digital record from the raw time record. It is an iterative process to find the thresholds for the two states, which I will describe briefly here.

After recording the time traces and constructing the amplitude histograms, we fit the histograms to a sum of Gaussians as shown in Figure 8.15. Because the two Gaussian functions are overlapping,

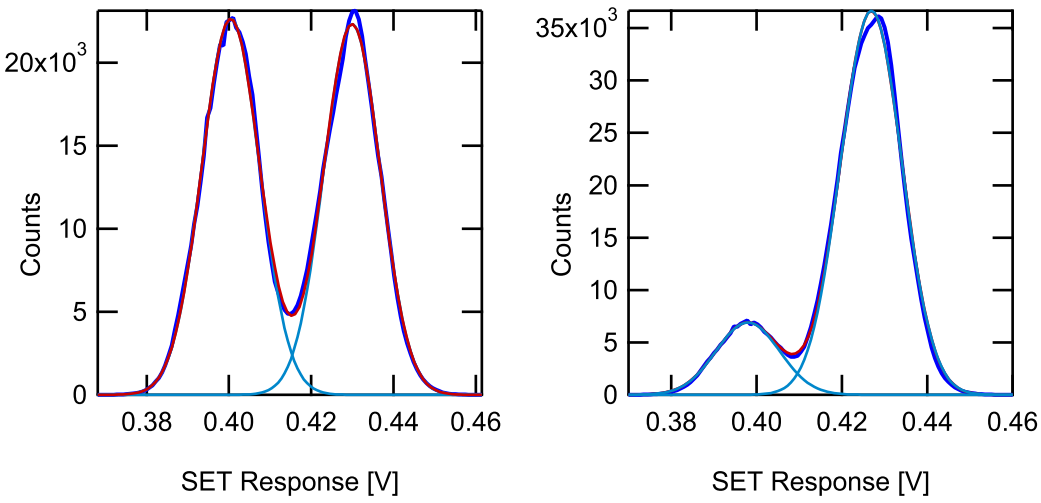

Figure 8.15: Amplitude histograms with fits to a sum of gaussians for two bias settings of the trap gate. Shown are the fits to the sum of the two Gaussians as well as the individual Gaussian curves to show the overlap between the two states.

we must use a statistical approach to sort out the events that fall in the overlapping region. Assuming

that the first event in the series starts out in the 0 state of the trap, we can calculate the probability that the next point in the time series is also in the down state, given its amplitude. We also calculate the probability that it is in the 1 state, given that the previous point was in the 0 state and compare these probabilities. We do the same for the trace starting in the 1 state, and the result is a double threshold. More simply stated, once the trap is determined to be in the 0 state, we record it as being in that state until the amplitude crosses above threshold T_0 as shown in Figure 8.16. Likewise, once

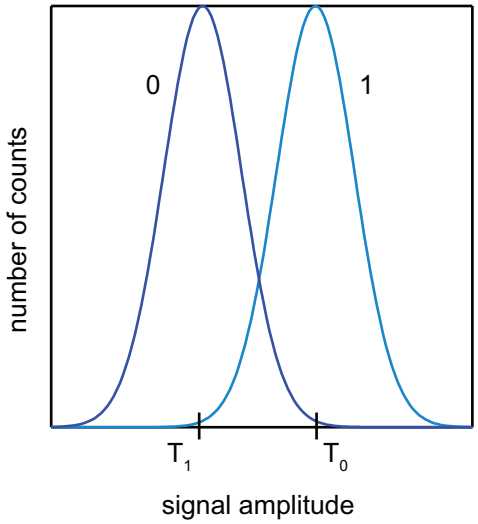

Figure 8.16: An example of a double histogram indicating the double threshold used for the Schmidt trigger. The left Gaussian is comprised of events recorded in the 0 state of the trap and the right Gaussian represents events in the 1 state. Once an event is recorded as being in the 0 state, for example, it will not be recorded as being in the 1 state until there is a recorded amplitude that lies above threshold T_0. Likewise, once an event is recorded in the 1 state, it will not be recorded as being in the 0 state until there is a recorded amplitude that lies below threshold T_1.

the trap is recorded to be in the 1 state, we continue to record it as being in the 1 state until the amplitude of the signal crosses below threshold T_1.

Given the amplitude histogram, we can calculate what these thresholds should be given the area under each gaussian, their mean values and standard deviations, and the lifetimes of each state. The goal of this problem is to find the lifetimes of each state, however, so of course we do not have that information. We could calculate the mean lifetimes if we knew the total number of transitions, but we also do not know that. What we do instead, is estimate the thresholds from the amplitude histograms. We use these to distribute the data into a digital time series consisting of 0's and 1's and then count the number of transitions. This gives a first estimate of the average lifetimes, which we can then use to calculate the thresholds. This process repeats and typically converges in five

iterations.

The result of this process is a digital record of the time trace, which is shown overlayed on the time trace shown above in Figure 8.17. The dwell times in each state are histogrammed and fit to a

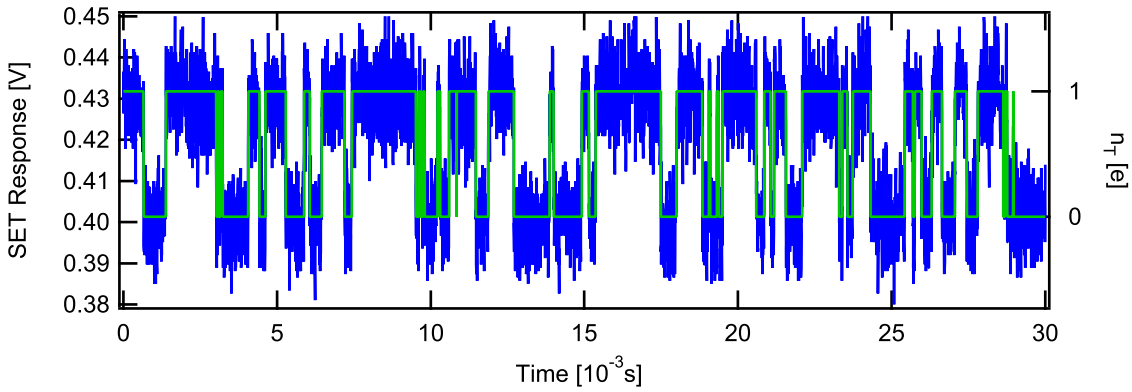

Figure 8.17: Raw time resolved random telegraph noise (blue) with digitized time trace overlayed showing the charge on the trap island (green).

decaying exponential to extract the average lifetime in each state. Examples of this are shown near trap charge degeneracy in Figure 8.18a and at a point far from trap degeneracy in Figure 8.18b. The fact that the decaying exponential fit agrees well with the data indicates strong agreement with the fact that the underlying physical process is Poissonian.

The measurement is repeated for many values of trap gate, in order to determine the gate dependence of the tunneling rates. The amplitude histograms for a measurement sequence, which recorded time traces over several periods in trap gate charge, are shown in Figure 8.19. This figure shows that the measurement process, including the performance of the SET, is stable over the course of the measurement. When there is a charge jump during the measurement process, it shows up in this type of diagram. One such example is shown in Figure 8.20. After the point of the charge jump, the SET is biased at a different operating point, and the data is thrown out. What is interesting to note is that when there is a charge jump, I have always observed that it occurs in the SET, and not in the trap device, meaning that the stability of the SET seems to be the limiting factor in the stability of these measurements.

The measured rates are plotted as a function of trap gate charge for three temperatures in Figure 8.22. Comparisons with theory are made for the 50 mK data in Figure 8.22. In these plots I show comparisons with a zero parameter theoretical model, with bands indicating the uncertainty in

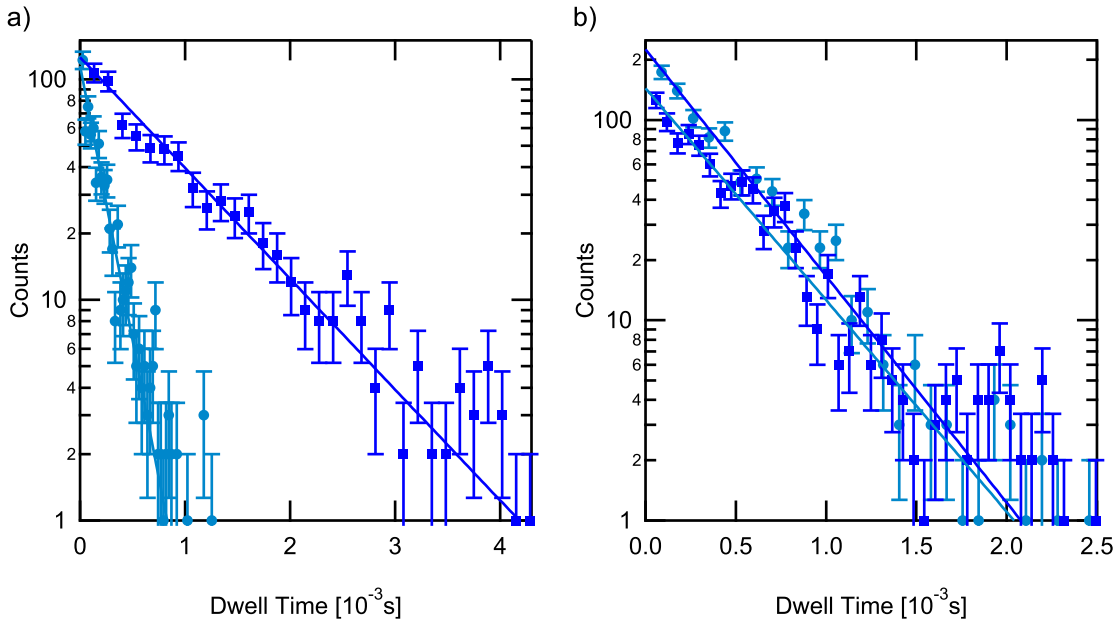

Figure 8.18: Dwell time histograms are constructed from digital time traces and fit to a decaying exponential. The squares represent counts in the 0 state and the circles represent the 1 state. a) Histogram constructed from a time trace away from the charge degeneracy point. b) Dwell time histogram constructed from a time trace measured near the charge degeneracy point of the trap.

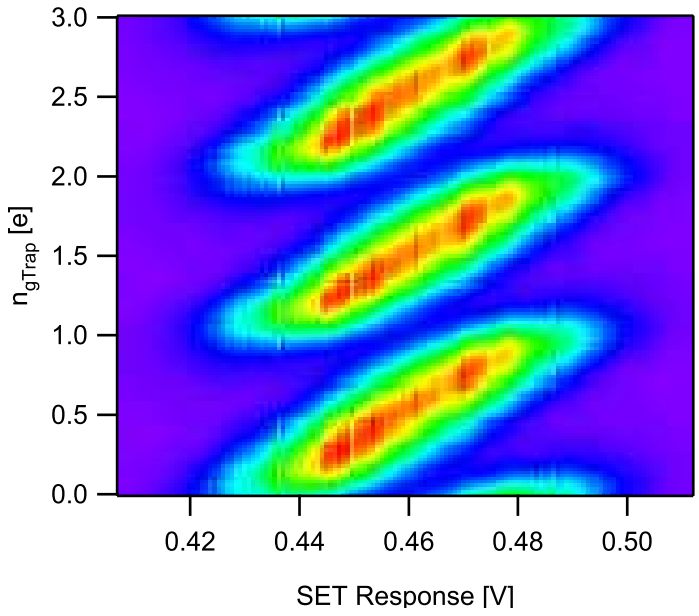

Figure 8.19: Amplitude histograms as a function of trap gate. The x-axis is the measured SET response, the y-axis is the trap gate bias, and the color scale represents the number of counts in each bin of SET response. The trap is stable and time domain measurements can be taken consistently over several periods in trap gate charge.

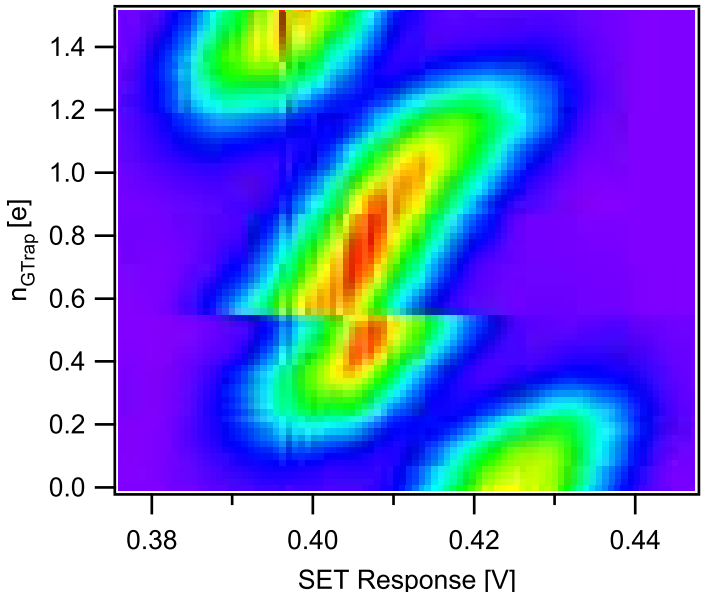

Figure 8.20: Amplitude histograms as a function of trap gate. The axes are the same as in Figure 8.19, but this time there was a jump in SET response. It is clear from looking at these graphs for many measurements that the SET is the most unstable element as the trap remains stable even if there is a jump in the SET.

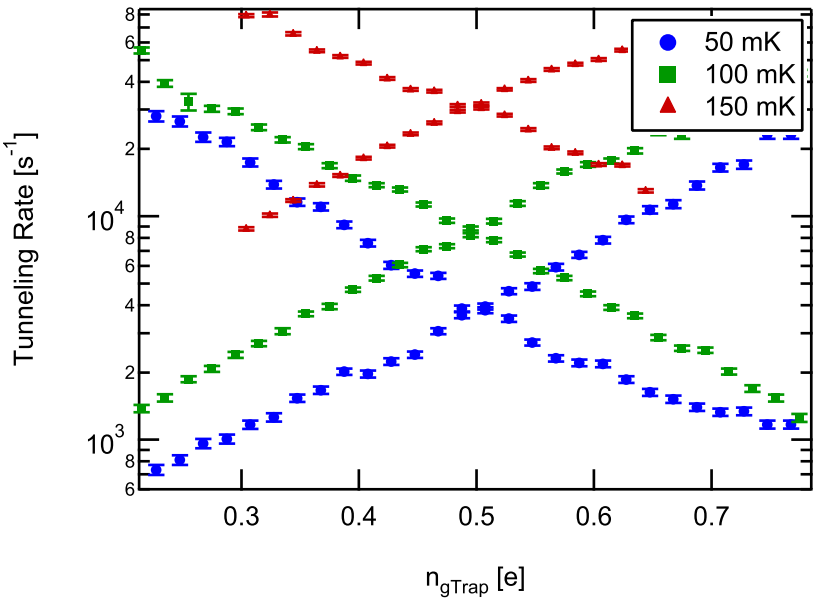

Figure 8.21: Tunneling rates measured in the trap as a function of trap gate at 50 mK, 100 mK, and 150 mK.

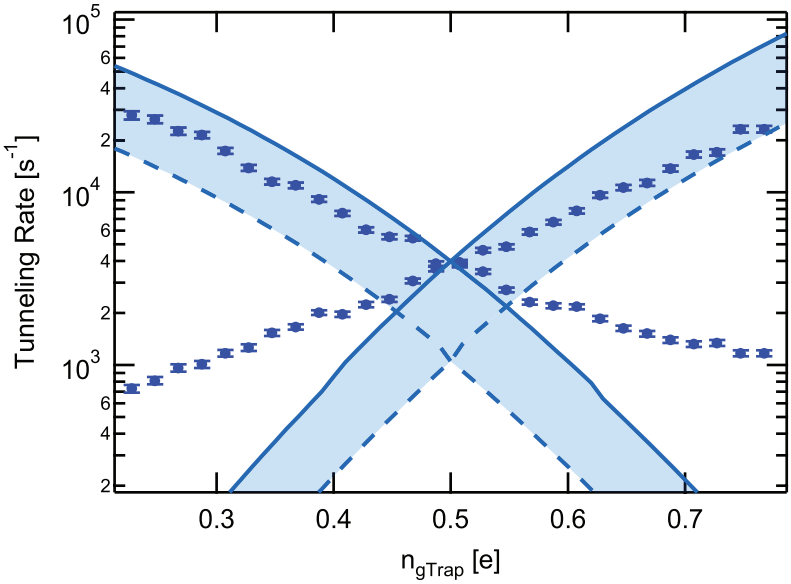

Figure 8.22: Tunneling rates for the trap as a function of trap gate. The shaded region bounded by the solid and dashed lines represents zero parameter calculations of the cotunneling rate over a range of the expected values for the parameters of the calculation.

the parameters of this model. Two main parameters were not possible to measure in this experiment: the charging energy of the island and the dimensionless conductance of the junctions, both of which set the overall scale of the tunneling rates. In addition to fabricating the device used for this experiment, I also fabricated test devices in which the trap island was shorted to the trap gate capacitor, turning the trap into an SET. From these test devices, I was able to put bounds on the expected parameters for this device as well as from viewing the sample after the measurements were taken. From this additional data, it is much more likely that the actual parameters for the measured device lie at the lower end of these bands. At 50 mK we see fairly good agreement with the cotunneling predictions for the rate to tunnel from the excited state to the ground state (the higher rate). This is especially true if we compare these with the predicted Orthodox theory curves at 50 mK, which are 14 orders of magnitude lower. The reverse rate, however, is not well described by the theoretical predictions. The measured temperature dependence of the rates is shown in Figure 8.23. Here, the agreement with the theoretical predictions is not as good, but still shows a qualitative agreement with the cotunneling theory as opposed to Orthodox theory. Still not well understood in either of these graphs, however, is the return tunneling rates. These are expected to be much lower than the measured values.

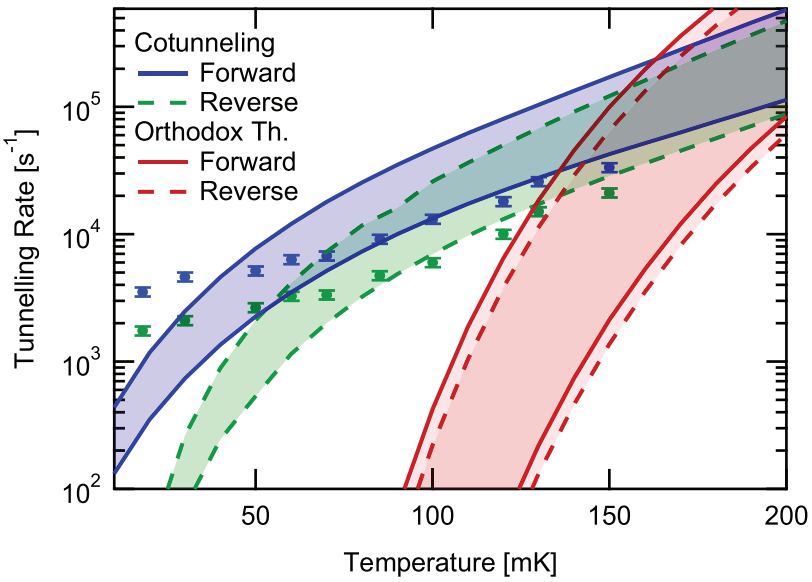

Figure 8.23: Tunneling rates for the trap as a function of temperature show a qualitative agreement with the cotunneling theory predictions. Both the data and the theoretical predictions are taken slightly away from the charge degeneracy point of the trap, at $n_{gTrap} = .55$. Orthodox theory rates are orders of magnitude lower for these temperatures.

As I mentioned earlier in this chapter, and discussed in detail in Chapter 5 in the discussion of cotunneling rates, it is necessary to consider the backaction of the SET when comparing the measured rates with expected theoretical values of the rates. These measurements of time resolved single tunneling events were possible because of the strong coupling between the trap island and the SET (in addition to the higher sensitivity of the SET). This increased coupling comes at a cost, however. The SET signal comes from having 10% of each trap electron coupled to the SET island. The SET is an electrometer, and there is a change in reflected power associated with any small changes in gate. Each electron tunneling onto the trap island is effectively a small gate on the SET, shifting the operating point slightly which allows us to conduct the measurement. The cost is that the trap is also measuring the SET. These devices are made up of the same parts and the problem is completely reversible. Each electron tunneling onto the SET shifts the operating point of the trap slightly. This reverse coupling is actually much stronger than the forward coupling of the trap electrons to the SET. Each SET electron is coupled with a strength of 20% to the trap island. This is the backaction of the SET onto the trap island, and this interaction modifies the rate curves.

With the second device, which is much more strongly coupled to the SET, we see a slight improvement in the agreement between the predicted theoretical rates and the measured rates if

we include the backaction of the SET into the calculation. The gate dependence of the rates is plotted in figure 8.24 along with theoretical bands of the calculations including the backaction. These calculations are done for the same range of device parameters as those shown in the graphs neglecting the backaction, and again, I expect that the parameters for this device lie in the lower range of these bands. The temperature dependence of the rates are shown with comparisons to

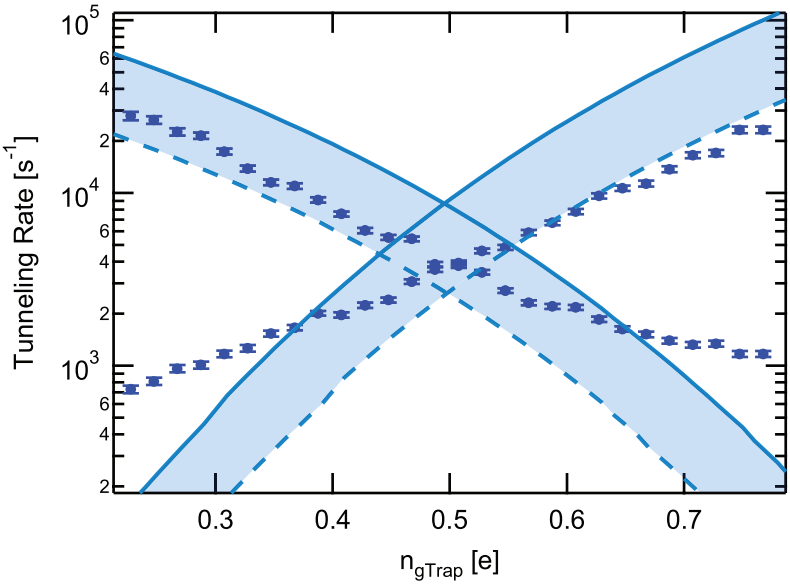

Figure 8.24: Tunneling rates for the trap as a function of trap gate. The shaded region bounded by the solid and dashed lines represents calculations of the cotunneling rate with no free parameters over the range of the expected values for the parameters of the calculation including contributions from the backaction of the SET.

theory in Figure 8.25. The shapes of the rate curves in both the gate and temperature dependence plots are more closely aligned with the data than those that did not account for the SET's backaction onto the trap. While the return rates are still not well explained by the theoretical predictions at low temperature, the forward rates and both rates at higher temperatures show excellent agreement with theoretical predictions. At increased temperatures, both the forward and reverse rates agree well with the theoretical predictions. Overall, the addition of the SET backaction only changes the predictions slightly, and the data show good agreement with both models, within the uncertainty of the model parameters.

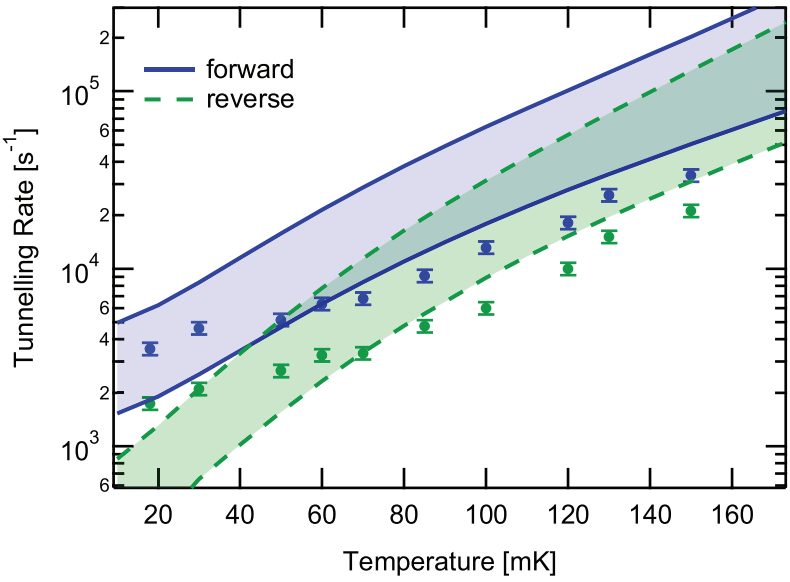

Figure 8.25: Tunneling rates for the trap are plotted as a function of temperature. We compare the data with a model of the cotunneling theory including the backaction of the SET with no free parameters. The data shows good agreement with the theory over a wide range of temperatures.

Chapter 9

Conclusions

9.1 Summary of Results

The work presented in this thesis is the time resolved measurements of single tunneling events in a metallic thin film circuit. I have designed and fabricated a circuit that has rates in the microsecond range that are tunable over almost two orders of magnitude. Using a RF-SET capacitively coupled to a single electron trap, I was able to time resolve single electron tunneling events. In the 400 microsecond average lifetime of the charge state with one excess electron on the trap island, 80 data points with SNR=10 can be obtained. In addition, I have made comparisons with both orthodox theory, or global rule, and cotunneling theory.

The measurements presented here are the first time resolved measurements of non-thermal tunneling events in a metallic system or quantum dot. They are also the first quantitative comparisons with cotunneling theory. Prior explorations of cotunneling dynamics [Kautz2000] disagreed with theory by many orders of magnitude and were complicated with the many-junction geometry and sensitivity to anomalous rare events. I was able to explore the dynamics of this circuit in several self-consistent ways. The first two methods were time averaged measurements that probed the underlying dynamics. This was first demonstrated in a qualitative way with measurements of the Coulomb staircase swept faster than the characteristic tunneling time. The hysteresis of the staircase measured as a function of the gate voltages illustrated the tunable nature of the rates, and the full two dimensional stability diagram provided a map of parameter space which allowed precise positioning for further measurements. I then performed pulsed gate measurements to obtain a more quantitative rate measurement that agreed favorably with cotunneling theory. In a second sample that had higher coupling to the SET island, giving higher measurement sensitivity, I was able to time

resolve the single electron tunneling events on the trap. I measured the tunneling rate as a function of gate and temperature, giving excellent agreement with cotunneling theory. It is well known that there is backaction from the SET which affects the measured device. We have assembled a preliminary model to incorporate this into our theoretical predictions, which changes the predictions and the agreement with the model only slightly. These measurements also demonstrate the possibility to extend this work to measurements of correlations and higher moments of charge fluctuations in metallic systems.

9.2 Future Work and Applications

A possibility of further research is to change the coupling to the SET and study the dynamical nature of the backaction of the SET. The mechanism for the backaction in the operation regime where the tunneling events in the SET are much more rapid than those in the trap has not been widely studied. In addition, the return rates of the trap at the lowest temperatures do not agree with the theoretical predictions. It is possible that more could be learned about this mechanism by modifying the strength of the interaction between the two circuits.

This research could also be further extended by studying the dynamics electron turnstile. This is a tunable circuit with four junctions and three islands, which can flow a current. The techniques developed for the trap experiments presented here can be applied to this similar circuit to do high-sensitivity low-noise measurements of single electron dynamics with application to current metrology and precision measurements. A quantum standard for the Ampere that depends only on quantum mechanics and the charge of the electron e could be accomplished with rapid counting of single electrons.

Appendix A

Fabrication Recipes

The recipes for the fabrication process outlined in Chapter 6 are presented here.

A.1 Wafer Preparation

1. Sonication in acetone 60s
2. Sonication in methanol 60s
3. Dry with N_2 and spin dry
4. Spin MMA-(8.5)MAA EL12 at 4000 rpm for 80s
5. Bake at 170 C for 5 minutes on hot plate fitted with aluminum plate to ensure temperature uniformity across the wafer. Cover with petri dish.
6. Cool 60 s on room temperature metal plate.
7. Spin PMMA 950K A3 at 3000 rpm for 80s
8. Bake at 170 C for 30 minutes (same setup as step 5)
9. Cool 60 s on room temperature metal plate.

A.2 Development

1. Prepare two small beakers:
   A. 30 mL MIBK:IPA 1:3 at 25° C
   B. 30 mL IPA at 25° C

2. Hold chip with tweezers, and gently agitate in beaker A for 48 s.
3. Quickly remove from beaker A, and gently agitate for 10 s in beaker B.
4. Gently dry with N_2 gas.

A.3 Aluminum Evaporation and Lift-off

1. Fill Plassys cold trap.
2. Load sample into load lock of Plassys.
3. Pump down chamber and load lock to $\sim 4 \times 10^{-7}$ Torr. This step takes approximately 1.5 hours.
4. Evaporate a few nm of titanium to lower the pressure to $\sim 2 \times 10^{-7}$ Torr.
5. Evaporate 35 nm aluminum at 0° from normal to the sample.
6. Wait 2 minutes
7. Oxidation step with Ar:O_2 85:15 at 3 Torr for 12 minutes.
8. Let the chamber pump back down. A second titanium deposition is optional here.
9. Evaporate 70 nm aluminum at 30° from normal to the sample. The angle here depends on the required shift.
10. Wait 2 minutes.
11. Remove sample from the Plassys and place in vertical sample holder in hot (70 C) acetone beaker on hot plate.
12. Squirt hot acetone on sample through a syringe removing the top layer of aluminum.
13. Sonicate sample in same aluminum bath for 30s.
14. Remove sample holder with tweezers from acetone bath, while spraying with fresh acetone from squirt bottle to prevent stray flakes of aluminum from finding their way back onto the silicon substrate.

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