

Free-standing silicon shadow masks for transmon qubit fabrication

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Nanofabrication techniques for superconducting qubits rely on resist-based masks patterned by electron-beam or optical lithography. We have developed an alternative nanofabrication technique based on free-standing silicon shadow masks fabricated from silicon-on-insulator wafers. These silicon shadow masks not only eliminate organic residues associated with resist-based lithography, but also provide a pathway to better understand and control surface-dielectric losses in superconducting qubits by decoupling mask fabrication from substrate preparation. We have successfully fabricated aluminum 3D transmon superconducting qubits with these shadow masks, and demonstrated energy relaxation times on par with state-of-the-art values.

Progress in superconducting circuits for quantum information technologies relies on the improvement of superconducting qubit lifetimes¹. One of the main sources of energy loss in these devices comes from the dielectric surfaces surrounding the Josephson junctions and associated superconducting circuitry. In particular, a number of experimental results attribute the majority of dielectric loss to one or several of the device-substrate, substrate-air, and device-air interfaces, rather than the bulk dielectrics^{2–11}.

State-of-the-art superconducting qubits are fabricated by patterning an organic resist with e-beam or optical lithography to create a liftoff mask, followed by shadow evaporation of the aluminum layer^{12–18}. Inevitably, this approach introduces contamination to the various interfaces⁵. This includes organic residues from the resist, contamination from the solvents that are required for the resist development after e-beam exposure, and those required for the lift-off process after metal deposition. Furthermore, degassing of the organic mask during metal deposition can lead to additional contamination.

In order to investigate the problems associated with residual contamination and eventually suppress it, we have developed a new nanofabrication technique for superconducting qubits (Fig. 1). Our technique replaces lift-off of an organic lithography layer with stencil lithography¹⁹ based on free-standing silicon shadow masks fabricated from silicon-on-insulator (SOI) wafers. Consequently, device substrate preparation becomes completely independent from the mask fabrication. As a result, the nanofabrication-related contamination is significantly reduced, and more important, controlled studies of surface dielectric losses as a function of surface preparation are now possible. Moreover, the inorganic mask is compatible with high-temperature processes, such as deposition of refractory metals and substrate annealing, which could be performed in situ. The silicon mask is free-standing, and thus can be removed from the target substrate at the end of the process and reused for subsequent depositions. It is also tension-free and therefore has higher mechanical stability relative to other possible stencil methods.

The masks were fabricated from 100 mm SOI wafers which consist of a 500 μm -thick substrate, 200 nm-thick SiO_2 layer

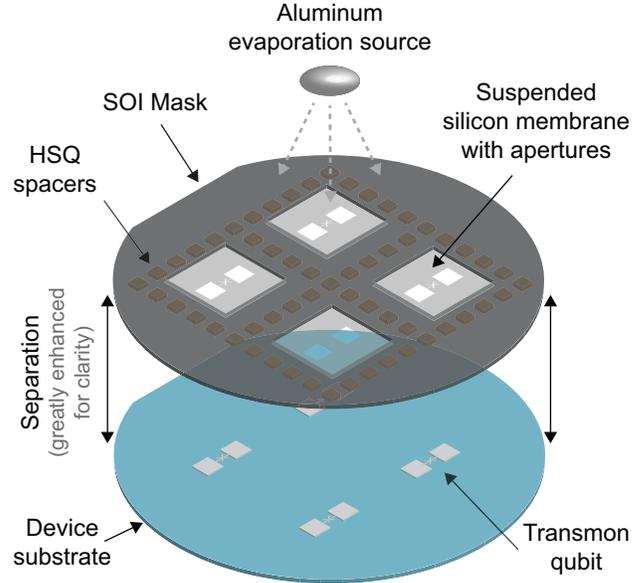


FIG. 1. Concept for nanofabrication of superconducting transmon qubits using free-standing silicon shadow masks (not to scale illustration). A silicon-on-insulator (SOI) wafer incorporates micrometer-thick suspended silicon membranes which contain apertures with submicron features. The stencil mask is placed on top of another wafer (device substrate). Aluminum is evaporated through it to create transmon structures on the device substrate. The micrometer-size crosslinked HSQ spacers control the distance between mask and device substrate. The mask is mechanically separated from the substrate at the end of aluminum deposition, leaving minimal nanofabrication-related residues. Here, the junction pattern has been caricatured for clarity.

and 5 μm -thick silicon top layer. The wafers incorporate a prefabricated array of 60, $(2.7 \times 8.6) \text{ mm}^2$, 5 μm -thick, suspended silicon membranes, where the silicon substrate and SiO_2 layer were completely etched away²⁰. A schematic cross-section of a single suspended silicon membrane is illustrated in Fig. 2(a). The fabrication process starts by creating spacers to control the distance between mask and device substrate. The wafer was spin coated at 1000 rpm for 2 minutes with hydrogen silsesquioxane (HSQ), which is a negative inorganic e-beam resist [Fig. 2(b)]. It was then patterned in a Vistec electron-beam pattern generator (EBPG-5000+) with a 100-keV electron beam and developed in MF-312 for

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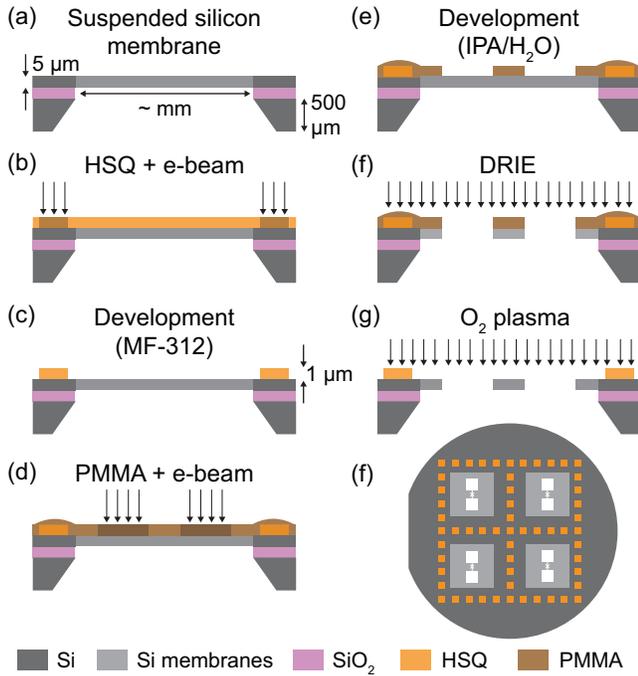


FIG. 2. (a-g) Schematic cross-section diagrams of the free-standing silicon shadow mask nanofabrication process (further described in the main text). (f) Top view schematic of the mask (not to scale).

5 minutes resulting in arrays of $(200 \times 200) \mu\text{m}^2$ and $1 \mu\text{m}$ -thick crosslinked HSQ spacers [Fig. 2(c,f)]. Transmon patterns were defined by apertures in the silicon membranes, created with another step of e-beam lithography. The wafer was spin coated with PMMA 950 A7 resist at 1500 rpm, baked for 5 min at 200°C , exposed with a 100-keV electron beam [Fig. 2(d)] and developed in IPA/ H_2O (3:1) at 6°C for 2 min [Fig. 2(e)]. The apertures were created in the suspended silicon membranes by the highly anisotropic deep-reactive-ion-etching (DRIE) BOSCH process²¹ [Fig. 2(e)]. As a last step, PMMA and other organic residues were removed from the mask with O_2 -plasma cleaning.

To demonstrate this new nanofabrication method, we focused on a mask design that is suitable for aluminum 3D transmon qubit¹⁴ fabrication. Fig. 3 is a simplified schematic describing the metal deposition method. The large rectangular apertures correspond to the capacitor pads and the narrow slits to the leads that will form the Josephson junction of the transmon. The deposition process requires the ability to tilt and rotate the mask-wafer stack with respect to the evaporation source, similarly to that employed in the so-called “Manhattan” process²². The first deposition is performed with the stage rotated parallel to the left slit ($\varphi = -45^\circ$) and tilted by angle θ , as shown in Fig. 3(a,b) and determined by considerations below. By selecting the width of the junction slits to be much smaller than the thickness of the suspended silicon membranes, and selecting θ accordingly, aluminum is deposited through the left slit and lands on the sidewalls of the right slit [Fig. 3(b)]. To accomplish this, the minimum tilt angle should satisfy $|\theta| > \arctan(w/t)$, where w is the width

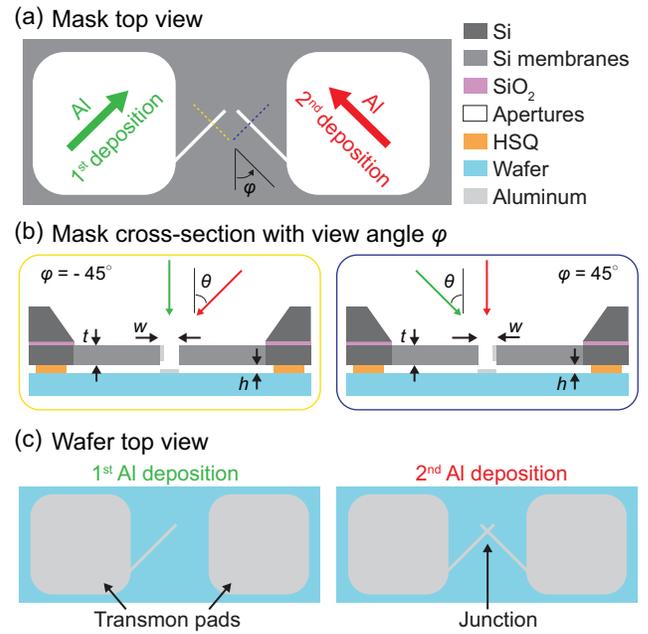


FIG. 3. (a) Simplified mask design schematic. The large apertures correspond to the transmon qubit capacitor pads and the narrow slits to the leads of the Josephson tunnel junction. The green and red arrows indicate orientation of the Al deposition steps. (b) Schematic cross-sectional view (not to scale) of the mask at two distinct positions and angles indicated by the yellow and blue lines. Green and red arrows indicate the tilt angle θ of the first and second deposition steps respectively. During the first deposition (green arrows), aluminum will only pass through the left narrow slit (yellow cross-section), and it will land on the sidewalls of the other aperture (blue cross-section). The reverse process occurs during the second deposition step (red arrows). (c) Top view schematic of the aluminum thin-film structure on the device wafer after each deposition step. The first Al deposition creates two capacitor pads and one thin lead, and the second Al deposition creates a second lead and contributes another layer to the capacitor pads. The Josephson junction is formed where these two leads cross.

of the slit and t the thickness of the silicon membrane. During the first deposition, the two capacitor pads and the first junction lead are formed, as shown in Fig. 3(c). An in situ oxidation step is then performed to create the tunnel barrier of the junction. A final (second) aluminum deposition with the stage rotated parallel to the right slit ($\varphi = 45^\circ$) and tilted by θ creates the second junction lead along with another aluminum layer on both capacitor pads [Fig. 3(c)].

Each fabricated mask contains multiple suspended silicon membranes patterned in that way. In Fig. 4(a-c), scanning electron microscopy (SEM) images of a single silicon membrane of a mask are shown. In every membrane, the capacitor pad apertures have dimensions of $(530 \times 480) \mu\text{m}^2$. We designed the width of the junction lead slits such as it gradually reduces in order to minimize possible conductive losses from otherwise long and narrow aluminum leads [Fig. 4(b)]. We vary the minimum width of the junction lead slits w , from 200 to $400 \mu\text{m}$, in order to create transmons with different junction area from the same mask. Narrower slits would require

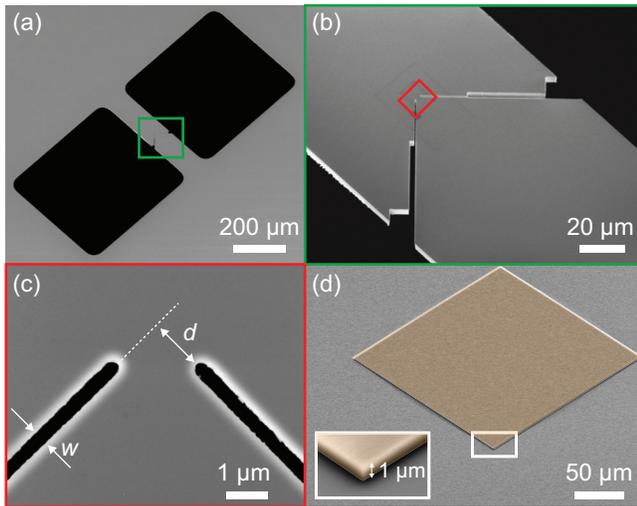


FIG. 4. (a-c) Scanning electron microscopy (SEM) images of a free standing silicon mask. Dark areas correspond to apertures and gray areas to suspended silicon. (d) False color SEM image of a $1\ \mu\text{m}$ thick crosslinked HSQ spacer.

further optimization of the DRIE process, as well as thinner silicon membranes²³. In order to increase the mechanical stability of the suspended silicon structure after etching, we opted to end the lead slits well before their crossing point. This imposes an additional condition that the tilt angle satisfies $|\theta| > \arctan(d/h)$ for the two aluminum junction leads to overlap, where h is the mask-substrate separation. The silicon membrane of $5\ \mu\text{m}$ thickness provides the necessary bending rigidity which further increases the mechanical stability of the suspended structure. Much thinner silicon would require a modified mask design with in-plane bridges across the slits. In Fig. 4(d) SEM image of a $(200 \times 200)\ \mu\text{m}^2$ and $1\ \mu\text{m}$ thick crosslinked HSQ spacer is shown. Arrays of such spacers across the mask are meant to define h and prevent possible adhesion of the mask on the device substrate due to Van der Waals forces.

With the mask shown in Fig. 4 we fabricated arrays of 3D transmons¹⁴ on $200\ \mu\text{m}$ -thick, 100-mm diameter c-plane sapphire wafers. The sapphire substrates were cleaned in N-methyl-2-pyrrolidone (NMP) at $90\ ^\circ\text{C}$ for 10 min, sonicated consecutively in NMP, acetone, and isopropyl alcohol (IPA) for 3 min each, and then dried with nitrogen. All metal deposition and oxidation steps were performed in a Plassys UMS300UHV multichamber electron-beam evaporation system without breaking vacuum in-between steps. After reaching a base pressure less than 5×10^{-9} torr, we evaporated 30 nm aluminum at $\varphi = -45^\circ$ and $\theta = 20^\circ$ at 1 nm/min rate. We then oxidized the aluminum in situ with a O_2/Ar (3:17) mixture for 15 min at 100 torr to create the tunnel barrier of the junction. A second evaporation of 40 nm aluminum was done at $\varphi = 45^\circ$ and $\theta = 20^\circ$. A final capping oxidation with a O_2/Ar (3:17) mixture for 5 min at 50 torr was then performed. The same mask was employed multiple times on different sapphire wafers. The wafers were diced in $(8 \times 3)\ \text{mm}^2$ chips, each containing a single transmon. To do so, we spin coated

the wafers with a SC-1827 photoresist layer at 1500 rpm for 2 min and baked it at $90\ ^\circ\text{C}$ for 9 min. This acts as protective layer against substrate debris damaging the devices during dicing. The resist was stripped at the end of the dicing process using sequentially NMP, acetone and IPA. Although the adoption of dicing resist is a common and convenient practice, it contradicts the purpose of our proposed technique which is to minimize fabrication residues, especially those coming from organic resist. However, the process of partitioning a wafer into smaller chips is independent of the fabrication of superconducting qubits at wafer-level, the main focus of our technique. The development of a reliable cleaving technique, which fundamentally does not require protective resist, would be essential for the full elimination of residues on the devices. Nonetheless, acknowledging the above limitation, we tested these devices in order to investigate whether our fabrication technique produces functional transmons.

Here, we present results for six transmons (A-F) derived from two independent sapphire wafers. In Fig. 5(a), optical images of qubit B are shown, where one can identify two aluminum layers that correspond to the two distinct evaporation steps. The double-lead pattern is the expected result of the double evaporation for a wide slit and does not affect the functionality of the devices. Nonetheless, the distance s between them provides an estimate for the effective mask-substrate separation of $h_{\text{eff}} = s/\tan\theta \approx 30\ \mu\text{m}$. This value is much larger than the thickness of the HSQ spacers ($1\ \mu\text{m}$). We attribute this to built-in residual compressive strain in the silicon device layer of the SOI wafer²⁴, which leads to buckling of the silicon membranes upon their release from the Si/SiO₂ substrate. Nevertheless, a notable characteristic of our mask design is that the junction overlap area is approximately independent of the mask-substrate separation, as it is only defined by the width of the two slits. This is contrary to the results of the Dolan-bridge technique¹², in which the junction area depends on both the mask substrate separation and the width of the slits. We further characterized the devices by taking atomic force microscopy (AFM) images of their junctions [Fig. 5(b)]. We believe that the asymmetry of the widths of the junction leads is due to misalignment from the intended rotation angle φ and fabrication variances of the mask aperture width. A characteristic of this technique is that the deposited metallic films have a softer edge profile compared to traditional lift-off-based fabrication technologies. This is primarily due to diffusion of the deposited material on the clean substrate^{19,25}.

We tested the devices in a dilution refrigerator with base temperature of $\approx 20\ \text{mK}$, adopting a standard circuit quantum electrodynamics (cQED) architecture in the dispersive readout regime²⁶. The chips were mounted in an aluminum 3D rectangular-waveguide cavity¹⁴ with fundamental mode at frequency $\omega_c/2\pi \approx 9.1\ \text{GHz}$. For qubits A, B, and C the external coupling rate of the cavity was set at $\kappa/2\pi = 5\ \text{MHz}$ and a waveguide Purcell filter (WR-90) with cut-off frequency at $\omega_c/2\pi \approx 6.6\ \text{GHz}$ was implemented to minimize qubit radiative losses²⁷. For qubits D, E, and F the coupling rate was set at $\kappa/2\pi = 0.38\ \text{MHz}$ minimizing the need for a Purcell filter. The measured properties for each qubit are presented

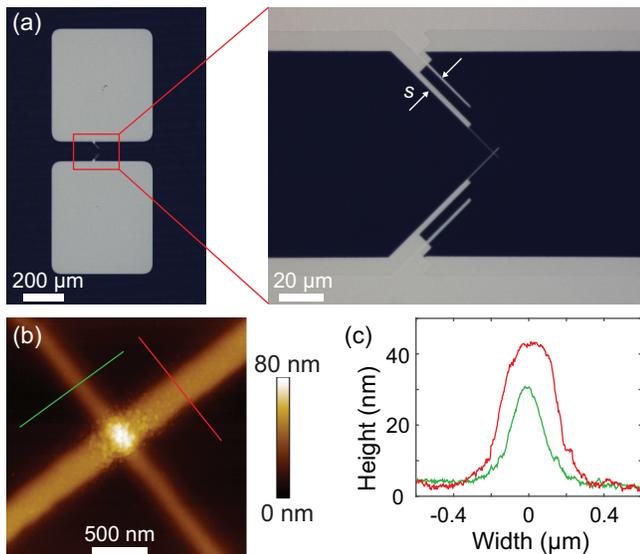


FIG. 5. (a) Optical images of a transmon qubit device fabricated using a free-standing silicon shadow mask (qubit B). The dark regions correspond to the sapphire substrate and the bright regions to deposited aluminum. (b) Atomic force micrograph (AFM) image of the Josephson junction (qubit C) formed at the crossing point of the two aluminum leads. (c) Height profile for each of the two aluminum leads at the cross-sections indicated by green and red color.

TABLE I. Measured transmon qubit parameters. From left to right, junction normal-state conductance G_N , qubit transition frequency ω_{ge} , anharmonicity $\alpha = \omega_{ge} - \omega_{ef}$, cross-Kerr χ , energy relaxation time T_1 , T_{2R} Ramsey and T_{2e} Hahn echo dephasing times. The fitting uncertainty for the decay times is up to $\pm 10\%$. When the range of variation between measurements exceeds the fitting uncertainty, it is given explicitly.

	G_N (mS)	$\omega_{ge}/2\pi$ (GHz)	$\alpha/2\pi$ (GHz)	$\chi/2\pi$ (MHz)	T_1 (μ s)	T_{2R} (μ s)	T_{2e} (μ s)
Qubit A	0.15	6.36	0.23	1.0	53-64	4	16
Qubit B	0.14	5.87	0.25	1.7	16	8-12	12-16
Qubit C	0.11	5.16	0.26	0.7	29	4-6	16-21
Qubit D	0.08	4.29	0.25	0.9	105-240	7-15	25
Qubit E	0.12	5.31	0.26	1.6	61	28	29
Qubit F	0.14	5.50	0.24	0.9	21	0.3	5

in Table I. The dispersion of T_1 times is comparable to what we have observed in transmons fabricated with standard techniques. The longest T_1 time, observed in qubit D, is on par with the state-of-the-art values²⁸. However, its performance fluctuated in time significantly, which necessitates additional investigation to understand. Moreover, further experimental studies are required to determine whether the energy relaxation properties of the devices are limited by surface dielectric losses⁶, by nonequilibrium quasiparticle excitations^{29,30} or other losses. The low T_{2R} Ramsey and T_{2e} Hahn echo dephasing times are attributed to residual thermal photon population in the 3D aluminum readout cavity modes³¹.

Single tunnel junctions have been previously fabricated with free-standing shadow masks based on silicon nitride

(Si_3N_4) membranes^{32,33}. However, in these efforts, the auxiliary probe-electrodes were fabricated in a separate step in advance. An advantage of free-standing membranes based on silicon, compared to Si_3Ni_4 , is that they are nominally free from residual in-plane tensile stress. As a result, silicon masks are mechanically robust enough to implement complex asymmetric aperture designs, allowing for better control of the Josephson junction area independent of mask-substrate separation. Additionally, large and small features can coexist on the same membrane. This provided us the means to fabricate tunnel junctions and the necessary auxiliary circuitry of a superconducting qubit device, such as the large capacitor pads of a 3D transmon qubit, using a single free-standing mask, reducing fabrication residues on the entire qubit device. Furthermore, our technique eliminates the need to align the tunnel junction with respect to the auxiliary circuitry. Inorganic shadow mask based on Ge/Nb bilayer have also been used for the fabrication of aluminum tunnel junctions by Welander *et al.*³⁴. In their work, Ge/Nb thin films are deposited and processed directly on the device substrate which could potentially introduce additional contamination relative to free-standing inorganic masks.

In conclusion, we have developed a nanofabrication technique for superconducting qubits that is based on inorganic free-standing silicon shadow masks, fabricated from SOI wafers. We fabricated aluminum 3D transmon qubits with these masks and performed preliminary observations of their coherence properties. Our work addresses the residual contamination drawbacks inherent to e-beam and optical lithography techniques, providing a solid experimental platform to better understand, control and potentially minimize surface-dielectric losses in planar superconducting circuits. This technique accomplishes full decoupling of the mask fabrication from device substrate preparation, and thus minimizes cross-contamination between the mask and the device substrate. Systematic investigations of the effect of substrate treatment on surface dielectric losses, without the restrictions imposed by organic resist processes are made possible. A key advantage of inorganic masks is their ability to sustain high metal deposition temperatures. To this end, free-standing silicon shadow masks hold promise as a suitable technique to fabricate high-quality superconducting qubits based on refractory materials with larger superconducting gap, such as niobium. In addition, high temperature substrate annealing⁸ can now be achieved in situ, under high vacuum, just before metal deposition, to further improve the surface properties of the device wafer. Finally, this technique is fully compatible with the fabrication of planar superconducting resonators, bringing to these necessary auxiliaries of tunnel junctions all of the aforementioned advantages.

We acknowledge insightful discussions with Michael Rooks, Michael Power, Shantanu Mundhada, Chan U Lei and Andrew Saydjari. Facilities use was supported by YINQE and the Yale SEAS cleanroom. This research was supported by the Army Research Office (ARO) under Grant No. W911NF-18-1-0212, and Grant No. W911NF-18-1-0020, and by the Multidisciplinary University Research Initiatives-Office of Naval Research (MURI-ONR) under Grant No. N00014-16-1-2270.

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